PERSONAL INFORMATION

Prof. Bijan Alizadeh, IEEE Senior Member

#320, School of Electrical and Computer Engineering, College of Engineering, University of Tehran, North Kargar Ave., Tehran 14395-515, Iran

+98-21-8204-5048 +98-912-770-7002

b.alizadeh@ut.ac.ir

https://dvdes.ut.ac.ir

https://www.linkedin.com/in/bijan-alizadeh-539b4825/?originalSubdomain=ir

https://scholar.google.com/citations?user=ivHILmEAAAAJ&hl=en

https://www.researchgate.net/profile/Bijan_Alizadeh

RESEARCH INTRESTS

- Embedded System Design Methodologies and Reconfigurable Computing (on FPGAs/ASICs)
- Formal and Semi-formal Verification Techniques as well as Post-silicon Debugging and Validation
- Hardware Accelerators for Brain-Inspired Computing and Neural Networks
- Hardware Security, High Level Optimization and Synthesis

EDUCATION AND TRAINING

September 1999 – January 2004

Ph.D. Degree

Electrical and Computer Engineering, University of Tehran, Iran

- **Thesis Topic:** High Level Formal Verification of Digital Circuits based on Property Checking

September 1996 – August 1999

M.Sc. Degree

Computer Engineering (Hardware), University of Tehran, Iran

- **Thesis Topic:** Implementation of Fault Tolerance Techniques in RISC Processors within Reliability Estimation

September 1992 – August 1996

B.Sc. Degree

Computer Engineering (Hardware), University of Tehran, Iran

- **Thesis Topic:** PCB-level Implementation of Digital Telephone Systems

PROFESSIONAL EXPERIENCE

August 2023 – Present

Full Professor and Head of Digital Systems Department

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Iran

- FPGA-based Hardware Accelerators
- Embedded Systems Design
- Large Language Model (LLM) for HDL Code Generation and Debugging
- Formal Methods for SoC Security
- Formal Verification and Debugging (Pre- and Post-Silicon) Techniques

August 2017 – August 2023

Associate Professor and Head oof Digital Systems Department (for two years)

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Iran

- Hardware Accelerated Embedded Platform for Real-Time Object Recognition using Convolutional Neural Network and Deep Learning
- FPGA-Based Implementation of Brillouin Frequency Shift in BOTDA and BOTDR Sensors
- Hardware-Software Co-design of Merging Units
- Formal Verification and Debugging (Pre- and Post-Silicon) Techniques
- Post Silicon Timing Error Recovery Techniques

July 2011 – August 2017

Assistant Professor and Head of Digital Systems Department (for two years)

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Iran

- Hardware Accelerator for Convolutional Neural Networks in Embedded Vision Applications
- Digital Design of Hardware Security Module (HSM)
- Formal Verification and Debugging (Pre- and Post-Silicon) Techniques
- High Level Synthesis and Optimization
- Timing Error Mitigation Techniques

September 2008 – June 2011

Project Assistant Professor

VLSI Design and Education Centre (VDEC), University of Tokyo, Tokyo, Japan

- Post-silicon Debug and Repair of Digital Systems
- Rapid Prototyping using FPGAs
- Verification and Debugging of Modern Processors

November 2007 – August 2008

Assistant Professor

School of Electrical Engineering, Sharif University of Technology, Tehran, Iran

- Reconfigurable Computing and Rapid Prototyping using FPGAs
- ASIC Chip (Digital) Design Methodologies

Nov. 2007 – November 2008

Vice-President for Research

Microelectronic Research and Development Centre, Tehran, Iran

- ASIC Chip (Digital) Design of Smartcards (Generation 2.5)

October 2006 – December 2007

Post-doctoral Research Associate

VLSI Design and Education Centre (VDEC), University of Tokyo, Tokyo, Japan

- Verification and Debugging of Modern Processors

March 2004 – September 2006

DSP Design Group Manager

Microelectronic Research and Development Centre, Tehran, Iran

- ASIC Chip (Digital) Design of WPAN System

January 2005 – September 2006

Assistant Professor

School of Electrical Engineering, Sharif University of Technology, Tehran, Iran

- ASIC Chip (Digital) Design Methodologies

October 2002 – February 2005

Formal Verification Group Manager

School of Electrical and Computer Engineering, College of Engineering, University of Tehran, Iran

- Development of Formal Verification Tool

August 1998 – September 2002

VLSI Design Group Manager

Emad Semicon. Corp., Tehran, Iran

- Physical Design of a Pager System
- ASIC Chip Design of Smartcards (Generation 2.0)
- Development of VHDL Simulator and Synthesis Tool

August 1996 – July 1998

Senior Digital Designer

DSP Group, University of Tehran, Tehran, Iran

- Rapid Prototyping of Digital Signal Processing (DSP) Applications

PERSONAL SKILLS

Organisational / managerial skills

- Microelectronic Research and Development Centre - Vice-President for Research (responsible for a team of 25 people)
- Microelectronic Research and Development Centre - DSP Group Manager (responsible for a team of 10 people)
- Emad Semicon. Corp - VLSI Design Group Manager (responsible for a team of 4 people)

Job-related skills

- Hands-on experience with Synopsys, Cadence and Mentor Graphics ASIC Design Tools such as First/SoC Encounter, Silicon Ensemble, Design Compiler, PrimeTime, DFTAdvisor, and FlexTest
- Hands-on experience with formal and semi-formal verification tools such as Formality, SMV, SLEC, VIS, and ABC
- System Level Design and Synthesis using BlueSpec, CatapultC and Chisel
- System Level Verification of Modern Processors using UCLID
- ASIC Chip Design and FPGA-based Embedded System Design
- Reconfigurable Computing using FPGA Platforms
- SAT-, MaxSAT- and SMT-based Debugging and Test Generation (MiniSat and Z3)

TEACHING EXPERIENCE

Springer 2011 – Spring 2024

Graduate Course:
- Formal Verification and Debugging of Digital Systems, School of ECE, University of Tehran, Iran.

Undergraduate Course:
- ESL Design Methodologies, School of ECE, University of Tehran, Iran.

Spring 2024

Undergraduate Course:
- Digital Logic Design, School of ECE, University of Tehran, Iran.

Spring 2011 – Spring 2012

Graduate Course:
- Automatic Synthesis of Digital Circuits, School of ECE, University of Tehran, Iran.

Fall 2011 – Fall 2024

Graduate Course:
- Methodologies for ESL Design Automation, School of ECE, University of Tehran, Iran.

Undergraduate Course:
- FPGA-based Embedded System Design, School of ECE, University of Tehran, Iran.

Fall 2024

Undergraduate Courses:
- Digital Logic Design, School of ECE, University of Tehran, Iran.
- Digital Systems I, School of ECE, University of Tehran, Iran.

Spring 2005 – Spring 2008

Graduate Course:
- ASIC Chip (Digital) Design, School of Electrical Engineering, Sharif University of Technology, Iran.

Undergraduate Course:
- Microprocessor and Microcontroller Systems, School of Electrical Engineering, Sharif University of Technology, Iran.

Fall 2005 – Fall 2008

Graduate Courses:
- Interface Circuit Design, School of Electrical Engineering, Sharif University of Technology, Iran.

- Embedded System Design, School of Electrical Engineering, Sharif University of Technology, Iran.

Undergraduate Course:
- Digital Logic Design, School of Electrical Engineering, Sharif University of Technology, Iran.

ASSOCIATE EDITOR

- IEEE Transactions on Circuits and Systems II – Express Briefs (TCAS-II), 2022-2023
- International Journal of Science and Technology (Scientia Iranica), 2018-Present

REVIEWING EXPERIENCE

- IEEE Transactions on Information Forensics and Security (TIFS Journal), 2018-Present
- IEEE Transactions on Instrumentation and Measurement (TIM Journal), 2020-Present
- IEEE Transactions on Circuits and Systems (TCAS-I & TCAS-II Journals), 2018-Present
- IEEE Transactions on Computers (TC Journal), 2017-Present
- IEEE Transactions on CAD (TCAD Journal), 2008, 2010-2013, 2017-Present
- IEEE Transactions on VLSI (TVLSI Journal), 2014-2015, 2016-Present

JOURNAL PUBLICATIONS

1. N. Aghapour, and B. Alizadeh, *Automatic Correction of Arithmetic Circuits in the Presence of Multiple Bugs by Groebner Basis Modification*, in ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 29, No. 5, Article No. 76, September 2024, pages 1-19.
2. A. Falahati, M. Shamirzaee, and B. Alizadeh, *An FPGA-based Hardware Architecture for P+M Class PMU Using Accuracy-Aware O-Spline Filter Selection and Modulation Detection*, in IEEE Transactions on Instrumentation and Measurement (TIM), Vol. 73, Article No. 9001408, May 2024, pages 1-8.
3. M. Moradi Shahmiri, and B. Alizadeh, *Concealing Exposed Circuit Features Through a MaxSAT-based Logic Locking Method*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 71, No. 4, April 2024, pages 2039-2043.
4. H. Hosseintalaee, A. Jahanian, and B. Alizadeh, *Systematic Trojan Detection in Crypto-Systems using the Model Checker*, in Journal of Circuits, Systems and Computers (JCSC), Vol. 33, No. 3, February 2024.
5. A. Sajadi, and B. Alizadeh, *A Resistant PUF-based Authentication Protocol Against Machine Learning Attacks*, in International Journal of electrical and Computer Engineering (IJECE), Vol. 21, No. 3, January 2024, pages 219-226.
6. M. Moradi Shahmiri, and B. Alizadeh, *HyLock: Hybrid Logic Locking based on Structural Fuzzing for Resisting Learning-based Attacks*, in ISC International Journal of Information Security (ISeCure), Vol. 15, No. 3, October 2023, pages 109-115.
7. A. Sajadi, A. Shabani, and B. Alizadeh, *DC-PUF: Machine Learning-Resistant PUF-based Authentication Protocol using Dependency Chain for Resource-Constrained IoT Devices*, in Elsevier Journal of Network and Computer Applications (JNCA), Vol. 217, August 2023, 103693.
8. B. Alizadeh, and M. Shiroei, *Automatic Correction of RTL Designs using a Lightweight Partial High-Level Synthesis*, in Integration, the VLSI Journal (INTEGRATION), Vol. 91, July 2023, pages 173-181.
9. F. Khormizi, and B. Alizadeh, *Vulnerability Analysis of Digital Circuits Against Capacitor-based Timing Hardware Trojan*, in Biannual Journal for CyberSpace Security (Monadi AFTA), Vol. 11, No. 1, September 2022, pages 18-25.
10. A. Ashtari, A. Shabani, and B. Alizadeh, *A Comparative Study of Machine Learning Classifiers for Secure RF*-PUF-based Authentication in Internet of Things, in Microprocessors and Microsystems – Embedded Hardware Design (MICPRO), Vol. 93, July 2022, Article 104600.
11. A. Ashtari, A. Shabani, and B. Alizadeh, *Mutual Lightweight PUF-based Authentication Scheme Using Random Key Management Mechanism for Resource-Constrained IoT Devices*, in ISC International Journal of Information Security (ISeCure), Vol. 14, No. 3, October 2022, pages 1-8.
12. F. Khormizi, A. Shabani, and B. Alizadeh, *Hardware Patching Methodology for Neutralizing Timing Hardware Trojans using Vulnerability Analysis and Time Borrowing Scheme*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 69, No. 6, June 2022, pages 2937-2941.
13. M. Sabri, A. Shabani, and B. Alizadeh, *SAT-based Integrated Hardware Trojan Detection and Localization Approach*

through Path Delay Analysis, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 68, No. 8, August 2021, pages 2850-2854.

14. A. Shabani, and B. Alizadeh, *Enhancing Hardware Trojan Detection Sensitivity using Partition-based Shuffling Scheme*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 68, No. 1, January 2021, pages 266-270.
15. B. Alizadeh, and Y. Abadi, *Incremental SAT-based Correction of Gate Level Circuits by Reusing Partially Corrected Circuits*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 67, No. 12, December 2020, pages 3063-3067.
16. A. Shabani, and B. Alizadeh, *PODEM: A Low-cost Property-based Design Modification for Detecting Hardware Trojans in Resource-Constraint IoT Devices*, in Elsevier Journal of Network and Computer Applications (JNCA), Vol. 167, October 2020, 102713.
17. M. Grailoo, and B. Alizadeh, *AIOSC: Analytical Integer Word-length Optimization Based on System Characteristics for Recursive Fixed-Point Linear Time Invariant Systems*, in International Journal of Engineering – Transactions A: Basics (IJE-A), Vol. 33, No. 7, July 2020, pages 1223-1230.
18. A. Azarmi, M. Emad, and B. Alizadeh, *FPGA-based Implementation of a Real-Time Object Recognition System using Convolutional Neural Network*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 67, No. 4, April 2020, pages 755-759.
19. A. Shabani, and B. Alizadeh, *PMTP: A MAX-SAT Based Approach to Detect Hardware Trojan using Propagation of Maximum Transition Probability*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 39, No. 1, January 2020, pages 25-33.
20. S. BeigMohammadi, and B. Alizadeh, *Combinational Hybrid Signal Selection with Updated Reachability Lists for Post-Silicon Debug*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 39, No. 1, January 2020, pages 272-276.
21. M. Abbasnejad, and B. Alizadeh, *FPGA-based Implementation of an Artificial Neural Network for Measurement Acceleration in BOTDA Sensors*, in IEEE Transactions on Instrumentation & Measurement (TIM), Vol. 68, No. 11, November 2019, pages 4326-4334.
22. M. Shiroei, B. Alizadeh, and M. Fujita, *Data-path Aware High Level ECO Synthesis*, in Integration, the VLSI Journal (INTEGRATION), Vol. 65, April 2019, pages 88-96.
23. M. Ahmadi, S. Salamat, and B. Alizadeh, *A Dynamic Timing Error Avoidance Technique Using Prediction Logic in High Performance Designs*, in IEEE Transactions on VLSI Systems (TVLSI), Vol. 27, No. 3, March 2019, pages 734-737.
24. B. Alizadeh, and R. Sharafinejad, *Incremental SAT-based Accurate Auto-correction of Sequential Circuits Through Automatic Test Pattern Generation*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 38, No. 2, February 2019, pages 245-252.
25. B. Alizadeh, and M. Shakeri, *QBF-Based Post Silicon Debug of Speedpaths under Timing Variations*, in IEEE Transactions on Circuits and Systems I (TCAS-I), Vol. 65, No. 12, December 2018, pages 4326-4335.
26. F. Refan, B. Alizadeh, and Z. Navabi, *Scalable Symbolic Simulation-Based Automatic Correction of Modern Processors*, in IEEE Transactions on VLSI (TVLSI), Vol. 26, No. 10, October 2018, pages 1845-1853.
27. M. Abbasnejad, and B. Alizadeh, *FPGA-Based Implementation of a Novel Method for Estimating the Brillouin Frequency Shift in BOTDA and BOTDR Sensors*, in IEEE Sensors Journal (JSEN), Vol. 18, No. 5, March 2018, pages 2015-2022.
28. R. Sharafinejad, B. Alizadeh, and Z. Navabi, *Automatic Correction of Dynamic Power Management Architecture in Modern Processors*, in IEEE Transactions on VLSI (TVLSI), Vol. 26, No. 2, February 2018, pages 308-318.
29. M. Grailoo, B. Alizadeh, and B. Forouzandeh, *Improved Range Analysis in Fixed-point Polynomial Datapath*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 36, No. 11, November 2017, pages 1925-1929.
30. SH. Moeini, B. Alizadeh, M. Emad, and R. Ebrahimpour, *A Resource Limited Hardware Accelerator for Convolutional Neural Networks in Embedded Vision Applications*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 64, No. 10, October 2017, pages 1217-1221.
31. F. Refan, B. Alizadeh, and Z. Navabi, *Bridging Pre-silicon and Post-silicon Debugging of Instruction-based Trace Signal Selection in Modern Processors*, in IEEE Transactions on VLSI (TVLSI), Vol. 25, No. 7, July 2017, pages 2059-2070.
32. M.R. Azarbad, and B. Alizadeh, *Scalable SMT-based Equivalence Checking of Nested Loop Pipelining in Behavioural Synthesis*, in ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 22, No. 2, March 2017, Article No. 22.
33. A.R. Mahzoon, and B. Alizadeh, *Systematic Design Space Exploration of Floating Point Expressions on FPGA*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 64, No. 3, March 2017, pages 274-278.
34. H. Mehri, and B. Alizadeh, *Analytical Performance Model for FPGA-based Reconfigurable Computing*, in Journal of Iranian Association of Electrical and Electronics Engineers (JIAEEE), Vol. 13, No. 4, January 2017, pages 1-13.
35. M. Ahmadi, B. Alizadeh, and B. Forouzandeh, *A Hybrid Time Borrowing Technique to Improve the Performance of Digital Circuits in the presence of Variations*, in IEEE Transactions on Circuits and Systems I (TCAS-I), Vol. 64, No. 1, January

2017, pages 100-110.

36. A.R. Mahzoon, and B. Alizadeh, *OptiFEX: A Framework for Exploring Area-Efficient Floating Point Expressions on FPGAs with Optimized Exponent/Mantissa Widths*, in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 25, No. 1, January 2017, pages 198-209.
37. M. Grailoo, B. Alizadeh, and B. Forouzandeh, *UAFEA: Unified Analytical Framework for IA/AA-based Error Analysis of Fixed-point Polynomial Specifications*, in IEEE Transactions on Circuits and Systems II (TCAS-II), Vol. 63, No. 10, October 2016, pages 994-998.
38. H. Mehri, and B. Alizadeh, *Genetic Algorithm Based FPGA Architectural Exploration using Analytical Models*, in ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 22, No. 1, December 2016, Article 13.
39. M. H. Haghbayan, and B. Alizadeh, *A Dynamic Specification to Automatically Debug and Correct Various Divider Circuits*, in Integration the VLSI Journal (INTEGRATION), January 2016, Vol. 53, pages 100-114.
40. H. Mehri, and B. Alizadeh, *Analytical Performance Model for FPGA-based Reconfigurable Computing*, in Microprocessors and Microsystems – Embedded Hardware Design (MICPRO), Vol. 39, No. 8, November 2015, pages 796-806.
41. M. Nejat, B. Alizadeh, and A. Afzali-kusha, *Dynamic Flip-Flop Conversion: A Time Borrowing Method for Performance Improvement of Low Power Digital Circuits Prone to Variations*, in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 23, No. 11, October 2015, pages 2727-2724.
42. S. Ghandali, B. Alizadeh, M. Fujita, and Z. Navabi, *Automatic High Level Data-flow Synthesis and Optimization of Polynomial Datapaths using Functional Decomposition*, in IEEE Transactions on Computers (TCOM), Vol. 64, No. 6, June 2015, pages 1579-1593.
43. B. Alizadeh, P. Behnam, and S. Sadeghi-kohan, *A Scalable Formal Debugging Approach with Auto-correction Capability based on Static Slicing and Dynamic Ranking for RTL Datapath Designs*, in IEEE Transactions on Computers (TCOM), Vol. 64, No. 6, June 2015, pages 1564-1578.
44. F. Farahmandi, and B. Alizadeh, *Groebner Basis Based Formal Verification of Large Arithmetic Circuits using Gaussian Elimination and Cone-based Polynomial Extraction*, in Microprocessors and Microsystems – Embedded Hardware Design (MICPRO), Vol. 39, No. 2, March 2015, pages 83-96.
45. B. Alizadeh, and P. Behnam, *Formal Equivalence Verification and Debugging Techniques with Auto-correction Mechanism for RTL Designs*, in Microprocessors and Microsystems – Embedded Hardware Design (MICPRO), Vol. 37, No. 8-D, November 2013, pages 1108-1121.
46. M. Mirzaei, M. Tabandeh, B. Alizadeh, and Z. Navabi, *A New Approach for Automatic Test Generation in Register Transfer Level Circuits*, in IEEE Design and Test of Computers, Vol. 30, No. 4, August 2013, pages 49-59.
47. B. Alizadeh, *Formal Verification and Debugging of Precise Interrupts on High Performance Microprocessors*, in ACM Transactions on Design Automation of Electronic Systems (TODAES), Vol. 17, No. 4, October 2012, pages 37-1:37-8.
48. B. Alizadeh, M. Mirzaei and M. Fujita, *Coverage Driven High Level Test Generation using a Polynomial Model of Sequential Circuits*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 29, No. 5, May 2010, pages 737-748.
49. B. Alizadeh, and M. Fujita, *Modular Data-path Optimization and Verification Based on Modular-HED*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 29, No. 9, September 2010, pages 1422-1435.
50. O. Sarbishei, M. Tabandeh, B. Alizadeh, and M. Fujita, *A Formal Approach for Debugging Arithmetic Circuits*, in IEEE Transactions on Computer-Aided-Design of Integrated Circuits and Systems (TCAD), Vol. 28, No. 5, May 2009, pages 742-754.
51. B. Alizadeh, and M. Fujita, *A Unified Framework for Equivalence Verification of Datapath-oriented Applications*, in IEICE TRANS. INF. & SYST., Vol. E92-D, No. 5, May 2009, pages 985-994.
52. B. Alizadeh, and M. Fujita, *Automatic Merge-point Detection for Sequential Equivalence Checking of System-level and RTL Descriptions*, Automated Technology for Validation and Analysis, Lecture Notes in Computer Science, Vol. 4762, November 2007, pages 129-144.
53. B. Alizadeh, and Z. Navabi, *Word Level Symbolic Simulation in Processor Verification*, IEE Journal Computers and Digital Techniques, Vol. 151, No. 5, September 2004, pages 356-366.
54. B. Alizadeh, and Z. Navabi, *A New High Level Model to Check CTL Properties in VHDL Environment*, Iranian Journal of Electrical and Computer Engineering, Vol. 1, No. 2, April 2003, pages 92-98.

CONFERENCE PUBLICATIONS

1. M. Moradi Shahmiri, and B. Alizadeh, *HyLock: Hybrid Logic Locking Based on Structural Fuzzing For Resisting Learning-based Attacks*, ISCISC 2023, Iran (to appear).

2. N. Aghapour, and B. Alizadeh, *Arithmetic Circuit Correction by Adding Optimized Correctors Based on Groebner Basis Computation*, ETS 2021, Belgium, pages 1-6.
3. M. Grailoo, B. Alizadeh, and T. Nikoubin, *ACPA: Exploiting Approximate Computing for High-Level Imprecision Optimization of Fixed-Point LTI Systems*, DCAS 2020, USA.
4. S. R. Sharafinejad, B. Alizadeh, and T. Nikoubin, *Formal Verification of Non-Functional Strategies of System-Level Power Management Architecture in Modern Processors*, DCAS 2020, USA.
5. A. Ashtari, A. Shabani, and B. Alizadeh, *A New RF-PUF based Authentication of Internet of Things using Random Forest Classification*, ISCISC 2019, IRAN, pages 21-26.
6. S. Salamat, M.R. Azarbad, and B. Alizadeh, *High Level Synthesis of Non-Rectangular Multi-Dimensional Nested Loops using Reshaping and Vectorization*, ICRC 2018, USA, pages 1-10.
7. H. Sabaghian, P. Behnam, B. Alizadeh, and Z. Navabi, *Reducing Search Space for Fault Diagnosis: A Probability-based Scoring Approach,* ISVLSI 2017, Germany, pages 545-550.
8. S. Salamat, M. Ahmadi, B. Alizadeh, and M. Fujita, *Systematic Approximate Logic Optimization Using Don't Care Conditions*, ISQED 2017, USA, pages 419-425.
9. S. BeigMohammadi, and B. Alizadeh, *Combinational Trace Signal Selection with Improved State Restoration for Post-silicon Debug*, DATE 2016, Germany, pages 1369-1374.
10. P. Behnam, B. Alizadeh, S. Taheri, and M. Fujita, *Formally Analysing Fault Tolerance in Datapath Designs using Equivalence Checking*, ASPDAC 2016, Macao, pages 133-138.
11. P. Behnam, and B. Alizadeh, *In-circuit Mutation-based Automatic Correction of Certain Design Errors using SAT Mechanisms*, ATS 2015, India, pages 199-204.
12. A. Mahzoon, and B. Alizadeh, *Multi-objective Optimization of Floating Point Arithmetic Expressions Using Iterative Factorization*, ISVLSI 2015, France, pages 243-248.
13. M. Ahmady, B. Alizadeh, and B. Forouzandeh, *A Timing Error Mitigation Technique for High Performance Designs*, ISVLSI 2015, France, pages 428-433.
14. A. Mahzoon, B. Alizadeh, and M. Fujita, *HOFEX: High Level Optimization of Floating Point Expressions for Implementation on FPGAs*, IWLS 2015, USA.
15. S. R. Sharafinejad, B. Alizadeh, and M. Fujita, *UPF-based Formal Verification of Low Power Techniques in Modern Processors*, VTS 2015, USA, pages 1-6.
16. F. Refan, B. Alizadeh, and Z. Navabi, *Signature Oriented Model Pruning to Facilitate Multi-Threaded Processors Debugging*, VTS 2015, USA, pages 1-6.
17. S. Ghandali, B. Alizadeh, and Z. Navabi, *Low Power Scheduling in High Level Synthesis using Dual-Vth Library*, ISQED 2015, USA, pages 507-511.
18. E. Qasemi, M. H. Shadmehr, B. Azizian, A. Samadi, S. Mozaffari, A. Shirian, and B. Alizadeh, *Highly Scalable, Shared Memory, Monte-Carlo Tree Search based Blokus Duo Solver on FPGA*, ICFPT 2014, China, pages 370-373.
19. H. Mehri, and B. Alizadeh, *An Analytical Dynamic and Leakage Power Model for FPGAs*, ICEE 2014, Iran, pages 300-305.
20. H. Haghbayan, B. Alizadeh, A. Rahmani, P. Liljeberg and H. Tenhunen, *Automated Formal Approach for Debugging Dividers Using Dynamic Specification*, DFT 2014, Netherlands, pages 264-269.
21. F. Farahmandi, B. Alizadeh, and Z. Navabi, *Effective Combination of Algebraic Techniques and Decision Diagrams to Formally Verify Large Arithmetic Circuits*, ISVLSI 2014, USA, pages 338-343.
22. V. Janfaza, P. Behnam, B. Forouzandeh, and B. Alizadeh, *A Low-power Enhanced Bitmask-dictionary Scheme for Test Data Compression*, ISVLSI 2014, USA, pages 220-225.
23. M. Nejat, B. Alizadeh, and A. Afzalikusha, *Dynamic Flip-Flop Conversion to Tolerate Process Variation in Low Power Circuits*, DATE 2014, Germany, pages 1-4.
24. S. Ghandali, B. Alizadeh, M. Fujita, and Z. Navabi, *RTL Datapath Optimization using System-level Transformations*, ISQED 2014, USA, pages 309-316.
25. S. Sadeghi-kohan, P. Behnam, B. Alizadeh, M. Fujita, and Z. Navabi, *Improving Polynomial Datapath Debugging with HEDs*, ETS 2014, Germany, pages 1-4.
26. P. Behnam, B. Alizadeh, and Z. Navabi, *Automatic Correction of Certain Design Errors using Mutation Technique*, ETS 2014, Germany, pages 1-2.
27. M. H. Haghbayan, B. Alizadeh, P. Behnam, and S. Safari, *Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism*, VLSI Design 2014, India, pages 80-85.

28. P. Behnam, H. Sabaghian, B. Alizadeh, K. Mohajerani, and Z. Navabi, *A Probabilistic Approach for Counterexample Generation to Aid Design Debugging*, EWDTS 2013, Russia, pages 1-5.
29. P. Behnam, B. Alizadeh, Z. Navabi, and M. Fujita, *Mutation-based Debugging Technique with Auto-correction Mechanism for RTL Designs*, SDD 2012, USA.
30. B. Alizadeh, and M. Fujita, *A Functional Test Generation Technique for RTL Datapaths*, HLDVT 2012, USA, pages 64-70.
31. S. Ghandali, B. Alizadeh, Z. Navabi, and M. Fujita, *Polynomial Datapath Synthesis and Optimization Based on Vanishing Polynomial over Z(2^m) and Algebraic Techniques*, MEMOCODE 2012, USA, pages 65-74.
32. B. Alizadeh, *A Formal Approach to Debug Polynomial Datapath Designs*, ASP-DAC 2012, Australia, pages 683-688.
33. B. Alizadeh, *A Symbolic Model-based Diagnosis with Auto-correction Framework for Arithmetic Circuits*, ASQED 2011, Malaysia, pages 195-202.
34. B. Alizadeh, and M. Fujita, *Early Case-splitting and False Path Detection to Improve High Level ATPG Techniques*, ISCAS 2011, Brazil, pages 1463-1466.
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