Negar Akbarzadeh

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Education

Ph.D.| SEPT. 2017-MARCH. 2024 | SHARIF UNIVERSITY OF TECHNOLOGY

- Major: Computer Engineering
- Minor: Computer System Architecture
- Overall GPA: 19.70/20
- Project: Designing a Scalable Memory System for GPUs

M.Sc. | SEPT. 2014-AUG. 2016 | SHAHID BEHESHTI UNIVERSITY

- Major: Electrical Engineering
- Minor: Electronics-Digital Systems
- Overall GPA: 19.37/20
- Project: Design and Implementation of Residue Number System Multiply and Multiply-add Units for Different Encodings

B.Sc. | SEPT. 2010-AUG. 2014 | SHAHID BEHESHTI UNIVERSITY

- Major: Electrical Engineering
- Minor: Electronics
- Overall GPA: 17.70/20
- Project: Object Detection and Tracking of a Ball in Animated Images

Honors & Awards

- Ranked 2nd highest GPA in B.Sc. at Shahid Beheshti University
- Ranked 1st highest GPA in M.Sc. at Shahid Beheshti University
- Admitted to M.Sc. in electrical engineering at Shahid Beheshti University as an exceptional student, exempt from "Iranian University Entrance Exam"
- Ranked 4th among 576 contestants in the "Iranian University Entrance Exam for Ph.D. Degree"
- Member of the National Elite Foundation for three years from 2018 to 2021

Publications

BOOK CHAPTERS

- M. Sadrosadati, A. Mirhosseini, N. Akbarzadeh, M. Modarressi, H. Sarbazi-Azad, Traffic-load-aware virtual channel power-gating in network-on-chips, Chapter 1, Advances in Computers, Elsevier, Vol.124, 2018, ISBN: 978-0-323-85688-1
- M. Sadrosadati, A. Mirhosseini, N. Akbarzadeh, H. Aghilinasab, H. Sarbazi-Azad, An efficient DVS scheme for on-chip networks, Chapter 2, Advances in Computers, Elsevier, Vol.124, 2018, ISBN: 978-0-323-85688-1

CONFERENCE PAPERS

- N.Akbarzadeh, S. Darabi, A. Gheibi-Fetrat, A. Mirzaei, M. Sadrosadati, H. Sarbazi-Azad, H3DM: A High-bandwidth High-capacity Hybrid 3D Memory Design for GPUs, SIGMETRICS 2024, Venice, Italy, 10-14 June, 2024
- A. Gheibi-Fetrat, N. Akbarzadeh, M.A. Khodabandelou, A. Ahmadi-Tonekaboni, S. Hessabi, H. Sarbazi-Azad, SmarTulip: A Turn-Free Low-Power and Low-Latency Network-on-Chip, Submitted to ASPLOS 2024, San Diego, USA, April 27- May 1, 2024
- S. Darabi, M. Sadrosadati, N. Akbarzadeh, J. Lindegger, S. Hosseini, J. Park, J. Luna, O. Mutlu, H. Sarbazi-Azad, Morpheus: Extending the last level cache in GPU systems with idle GPU cores' resources, IEEE/ACM MICRO-2022, 1-5 October 2022, Chicago, USA
- N. Akbarzadeh, S. Timarchi, A. Hamidi, Efficient multiply-add unit specified for DSPs utilizing low-power pipeline modulo 2n+ 1 multiplier, 2015 9th Iranian conference on machine vision and image processing (MVIP), pp. 120-123, 18-19 Nov. , 2015
- S. Timarchi, N. Akbarzadeh, A. Hamidi, Maximally redundant high-radix signed-digit residue number system, 2015 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS), 7-8 October, 2015
- A. Hamidi, S. Timarchi, N. Akbarzadeh, Block-based hardware implementation of FAST corner detection algorithm, The first international conference of modern research engineers in electricity and computer, 12 May, 2016
- F. Ghahari, N. Akbarzadeh, K. Jafari, R. Gholamzadeh, Design and Finite Element Analysis of a MEMS Capacitive Microphone, The first international conference of modern research engineers in electricity and computer, 12 May, 2016
- A. Hamidi, S. Timarchi, N. Akbarzadeh, Comparison and software simulation of various feature descriptors, The first international conference of modern research engineers in electricity and computer, 12 May, 2016

JOURNAL PAPERS

- N. Akbarzadeh, M. Sadrosadati, A. Gheibi-Fetrat, H. Sarbazi-Azad, Designing a High-bandwidth and High-capacity Memory for GPUs, Submitterd to ACM Transactions on Architecture and Code Optimization (TACO), Under Review
- A. Gheibi-Fetrat, N. Akbarzadeh, H. Sarbazi-Azad, Tulip: Turn-Free Low-Power Network-on-Chip, IEEE Computer Architecture Letters, Vol.23, No.1, pp. 5-8, Jan.-June 2024
- H. Bakhishi, N. Akbarzadeh, M. Sadrosadati, H. Sarbazi-Azad, Improving GPGPU Performance Through Efficient Use of Memory Controllers, Vol.18, No.2, 2020
- S. Darabi, E. Yousefzadeh, N. Akbarzadeh, H. Falahati, P. Lotfi-Kamran, M. Sadrosadati, H. Sarbazi-Azad, OSM: Off-chip shared memory for GPUs, Vol.33, No.12, pp.3415-3429, 2022
- N. Akbarzadeh, S. Timarchi. Modulo 2"+ 1 Multiplication and Multiply-Accumulate Units for Digital Signal Processor, Journal of Signal and Data Processing (JSDP), Vol.15, No.1, pp. 127-138, 2018
- S. Timarchi, N. Akbarzadeh, Area-Time-Power Efficient Maximally Redundant Signed-Digit Modulo 2n – 1 Adder and Multiplier, Circuits, Systems, and Signal Processing, Vol.38, No.5, pp. 2138-2164, 2019

Experiences

TEACHING EXPERIENCE

- Teaching "Computer Structure and Organization" course at Sharif University of Technology for 2 terms

TEACHING ASSISTANTSHIPS UNDER PROF. SARBAZI-AZAD

- Assisted in teaching "Computer Architecture" for 4 terms
- Assisted in teaching "Computer Structure and Organization" for 4 terms
- Assisted in teaching "Advanced Computer Architecture" for 1 term
- Assisted in teaching "Interconnection Networks" for 1 term
- Assisted in the "Laboratory of Computer Architecture" for 3 terms

TEACHING ASSISTANTSHIPS UNDER DR. HEMMATYAR

- Assisted in teaching " Wireless Communication" for 1 term
- Assisted in teaching "Logic Circuits" for 1 term
- Assisted in teaching "Presentation of Scientific and Technical Topics" for 2 terms

TEACHING ASSISTANTSHIPS UNDER DR. TIMARCHI

- Assisted in teaching "Computer Architecture" for 4 terms
- Assisted in teaching " Logic Circuits " for 1 term
- Assisted in the “Laboratory of Logic Circuits" for 4 terms

INDUSTRIAL EXPERIENCE

- Worked as a backend and Android developer at Ghalamchi Educational-Cultural Institute for a duration of 4 years

Softwares & Languages

DISCRETE ELECTRONIC CIRCUIT DESIGN	ISE, Proteus, Pspice, Codevision, Orcad, Quartus
SPECIALIZED ELECTRONIC DESIGN	Cadence, Synopsis Design Vision, Modelsim (VHDL)
WEB & MOBILE DEVELOPMENT	Android Studio (JAVA), HTML, CSS, Bootstrap, SQL, ASP.NET
OTHERS	Matlab, Microsoft Visual Studio (C++/ C#/ OpenCV), Ansys (Mechanical APDL), Silvaco (Atlas/ Athena)

Academic Projects

- Detecting and tracking objects in live webcam feed utilizing OpenCV and C++
- Hardware description of Peterson Architecture using VHDL
- Implementation of MANO architecture on printed circuit board
- Implementing various Parallel Prefix adder structures using Cadence Virtuoso
- Implementation of various Adders and Multipliers in Residue Number Systems (RNS) using VHDL and Synopsis Design Vision
- Configuring LCD on Spartan 3e FPGA board using VHDL
- Initializing a mouse via RS232 interface on Spartan 3e FPGA board using VHDL
- Implementing Pannotia game on Spartan 3e FPGA board with VGA display using VHDL
- Executing multiple projects in MATLAB, exploring various image processing algorithms
- Simulating and analysis of finite element models of MEMS capacitive microphones using Ansys Mechanical APDL
- Simulating and analysis of motor drive circuits in Matlab Simulink
- Simulating MOSFET transistors using Silvaco Athena/Atlas software tool
- Simulating various analog circuits in PSpice, including MOSFET cascaded and differential amplifiers
- Developing an engineering calculator using C and C#
- Implementing several algorithms using MIPS assembly language