Kamyar Givak

Ph.D. IN COMPUTER ENGINEERING - COMPUTER SYSTEMS ARCHITECTURE

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Computer Arithmetic, Stochastic and approximate Computing, Low-Power Design, Machine Learning

Education

Ph.D. in Computer Engineering - Computer Systems Architecture

Tehran, Iran

UNIVERSITY OF TEHRAN 2016 - 2023

THESIS: DESIGNING EFFICIENT ARCHITECTURE FOR MACHINE LEARNING APPLICATIONS BASED ON STOCHASTIC COMPUTING

RESEARCH OBJECTIVES:

- DESIGNING ULTRA-EFFICIENT HARDWARE MODULES BASED ON REQUIRED COMPUTATIONS IN MACHINE LEARNING APPLICATIONS.
- · STUDY THE COMPUTATION PATTERNS AND REQUIREMENTS IN SEVERAL MACHINE LEARNING TASKS.
- · INTRODUCE A GENERIC HARDWARE DESIGN SCHEME WITH THE COMBINATION OF RESIDUE NUMBER SYSTEMS AND DETERMINISTIC APPROACHES TO STOCHASTIC COMPUTING.

TAKEN MODULES: PERFORMANCE EVALUATION OF COMPUTER SYSTEMS, ADVANCED COMPUTER MATHEMATICS, ADVANCED REAL-TIME SYSTEMS, CHIP MULTIPROCESSOR ARCHITECTURES, EMBEDDED SYSTEMS PROCESSING ELEMENTS, MULTI-CORE EMBEDDED SYSTEMS.

M.Sc. in Computer Engineering - Computer Systems Architecture

Isfahan, Iran 2014 - 2016

ISFAHAN UNIVERSITY OF TECHNOLOGY

THESIS: A HIGH-PAYLOAD STEGANOGRAPHY TECHNIQUE USING NON-BINARY SPACES

RESEARCH OBJECTIVES:

- DESIGNING A STEGANOGRAPHY METHOD FOR IMAGES WITH HIGH EMBEDDING EFFICIENCY.
- THE METHOD OFFERS MINIMUM IMPACT ON VISUAL QUALITY OF THE IMAGE.
- IS ROBUST AGAINST CA-HCF-COM ATTACK.

MODULES: DIGITAL SIGNAL PROCESSING, NETWORK SECURITY, ADVANCED COMPUTER ARCHITECTURE, VHDL, EXPERT SYSTEMS, COMPUTER ARITHMETIC, SPECIAL TOPICS IN COMPUTER (DECISION SUPPORT SYSTEMS)

B.Sc. in Computer Engineering - Hardware

Tehran, Iran

K.N.Toosi University of Technology

2006 - 2012

FINAL PROJECT: DESIGN AND IMPLEMENTATION OF A DIGITAL NOISE GENERATOR

FINAL PROJECT OBJECTIVES:

- DESIGNING A NOISE GENERATOR WITH DIFFERENT DISTRIBUTIONS AND IMPLEMENTING THEM USING VHDL.
- DESIGN A PCB FOR A XILINX SPARTAN-II FPGA WITH SEVERAL I/O INCLUDING SEVERAL ADCS AND DACS AND FABRICATING THE CIRCUIT.

SELECTED MODULES: ADVANCED PROGRAMMING, SYSTEM ANALYSIS, OPERATING SYSTEMS, DATA COMMUNICATIONS, COMPUTER NETWORKS, LINEAR CONTROL, ELECTRONIC CIRCUITS, ELECTRONICS II, DIGITAL ELECTRONICS, VLSI SYSTEMS DESIGN, DIGITAL INTEGRATED CIRCUITS DESIGN, PARALLEL PROCESSING, COMPUTER ARCHITECTURE, DIGITAL DESIGN, MICROPROCESSORS, AI

Research Interests

- · Computer architecture
- · Computer arithmetic
- · Low-energy and resilient hardware designs

- · Stochastic & Unary computing
- · Ultra-low-power embedded systems
- · Hardware accelerator design

Honors & Awards

Short Term Collaboration Grant

Barcelona, Spain

EUROLAB4HPC (A HORIZON 2020 FUNDED PROJECT)

2020

Patents.

Method and Architecture for Accelerating Deterministic Stochastic Computing using Residue Number System

Mohammadhassan Najafi, Kamyar Givaki, Seyed Reza Hojabrossadati, MH Gholamrezayi, Ahmad Khonsari, Saeid Gorgin, Dara Rahmati

US Patent, Pub. number: US-20210241085-A1

2021

Embedded Stochastic-Computing Accelerator for Convolutional Neural Networks

Mohammadhassan Najafi, Seved Reza Hojabrossadati, Kamyar Givaki, SM Reza Tayaranian, Parsa Esfahanian, Ahmad Khonsari, Dara Rahmati

US Patent, Pub. number: US-20210256357-A1

2021

Publications_		
	ber System Design Approach for Ultra-Low Power Arithmetic Circuits Based on Deterministic Bit-streams	
	isari, MH Gholamrezaei, Saeid Gorgin, M Hassan Najafi	
IEEE Transactions on Comp	uter-Aided Design of Integrated Circuits and System	202
Hardware Efficient FIR Filte	er Architectures Using Accurate Unary Stochastic Computing	
KAMYAR GIVAKI, AHMAD KHON	isari, MH Gholamrezaei, Dara Rahmati, Saeid Gorgin	
IEEE 40^{th} International Co.	nference on Computer Design (ICCD)	202
High Performance Determin	nistic Stochastic Computing Using Residue Number System	
Kamyar Givaki, Reza Hojabr	r, MohammadHosein Gholamrezaei, Ahmad Khonsari, Saeid Gorgin, Dara Rahmati, M. Hassan Najafi	
IEEE Design & Test, Volume	38, Issue 6	202
On the Resilience of Deep Le	earning for Reduced-voltage FPGAs	
KAMYAR GIVAKI, BEHZAD SALA	ami, Reza Hojabr, SM Reza Tayaranian, Ahmad Khonsari, Dara Rahmati, Saeid Gorgin, Adrian Cristal, Osman S Unsal	
28^{th} Euromicro Internation	nal Conference on Parallel, Distributed and Network-Based Processing (PDP)	20.
TaxoNN: A Light-Weight Acc	elerator for Deep Neural Network Training	202
-	i, Kossar Pourahmadi, Parsa Nooralinejad, Ahmad Khonsari, Dara Rahmati, M. Hassan Najafi	
IEEE International Symposium on Circuits and Systems (ISCAS)		
SkippyNN: An Embedded St	ochastic-Computing Accelerator for Convolutional Neural Networks	202
	i, SM Reza Tayaranian, Parsa Esfahanian, Ahmad Khonsari, Dara Rahmati, M Hassan Najafi	
56^{th} Annual Design Autom	nation Conference 2019	
		201
-	rems to Accelerate Deterministic Bit-stream Multiplication r, M Hassan Najafi, Ahmad Khonsari, M Hossein Gholamrezayi, Saeid Gorgin, Dara Rahmati	
	nference on Application-specific Systems, Architectures and Processors (ASAP)	201
-	pedance estimation in power system	
KAMYAB GIVAKI, SALEH SEYEDZ	ADEH, KAMYAR GIVAKI	
8 th Renewable Power Gen	eration Conference (RPG)	201
Skills		
Technologies	Git, SVN, Kubernetes, Docker.	
Programming	C, C++, C#, Python, VHDL, Verilog.	
Frameworks and Libraries	Scikit-learn, TensorFlow, Keras, Pytorch, NLTK, SpaCy, Gym, CUDA, OpenMP.	
Tools	Synopsys Design Compiler, Vivado Design Suite, ModelSim, HSpice, Matlab, Visual Studio, Gem5.	
os	Linux(RHEL/Centos/Ubuntu), Microsoft Windows	
Interpersonal Skills	Problem-solving, Teamwork, Leadership, Focus, Public speaking, Active listening, Management	

References_

Dr. Ahmad Khonsari, Associate professor

Other Skills MS VISIO, Latex

ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT, UNIVERSITY OF TEHRAN, TEHRAN, IRAN

Languages English TOEFL Score: 89 (*Reading: 26, Listening: 28, Speaking: 14, Writing: 21*).

Dr. M. Hassan Najafi, Assistant professor

SCHOOL OF COMPUTING AND INFORMATICS, UNIVERSITY OF LOUISIANA AT LAFAYETTE, USA

<u>Dr. Dara Rahmati</u>, Assistant professor

FACULTY OF COMPUTER SCIENCE AND ENGINEERING, SHAHID BEHESHTI UNIVERSITY, TEHRAN, IRAN

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