Curriculum Vitae

Personal Information:

Name: Dara Rahmati

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Address: Room 230, Faculty of Computer Science and Engineering, Shahid Beheshti University, Daneshjou Boulevard, Velenjak, Tehran, Iran.

Profession:

- Assistant Professor at the Faculty of Computer Science and Engineering, Shahid Beheshti University (https://cse.sbu.ac.ir/~d_rahmati), 2019-now.
- Post Doctoral Researcher at the Institute for Research in Fundamental Sciences (IPM) (http://www.ipm.ir), School of Computer Science (http://cs.ipm.ac.ir), Tehran, Iran, since, 2015-2019.
- Head of the High Performance Computing Center (HPC Center), IPM, Tehran, Iran. (http://hpc.ipm.ac.ir) 2017-now.
- Embedded System Designer/Developer/Consultant, Shetab Saman Co. (2015-now), (Previously, CEO Shetab Saman Co. 2004-2015) . (http://www.shetabsaman.com)

Education:

- Ph.D. in Computer Engineering, Sharif University of Technology, Tehran, Iran, 2012.
  HPCAN (High Performance Computing and Network Laboratory), (http://hpcan.ce.sharif.ir)
  Thesis Title: Analytical Modeling and Performance Evaluation for Networks-on-Chip with Quality-of-Service Guarantee.
  Thesis Grade: Excellent
- M.Sc. in Computer Engineering – Hardware, University of Tehran, Tehran, Iran, 2001.
  Thesis Title: "A Hybrid Interpreted-Compiled Code VHDL Event-Driven Simulator with Extensibility", Thesis Grade: 19.75/20, GPA: 16.50/20.
- B.Sc. in Computer Engineering - Hardware, University of Tehran, Tehran, Iran, 1998.
  Final project: "30 Channels PC Sound Card", GPA: 16.83/20.

Internship:

- **Internship** at the Laboratoire des Systèmes Intégrés (LSI) (https://lsi.epfl.ch), at the École Polytechnique Fédérale de Lausanne (EPFL) (http://www.epfl.ch), Switzerland. Also **a collaboration** with the company iNoCs SaRL (http://www.inocs.com), headquartered in Lausanne, Switzerland, from January 1st, 2009 until August 31st, 2009.

Patents:

- Embedded stochastic-computing accelerator architecture and method for convolutional neural networks, Mohammadhassan Najafi, Seved Reza Hojabrossadati, Kamyar Givaki, SM Reza Tayaranian, Parsa Esfahanian, Ahmad Khonsari, Dara Rahmati,
  US Patent App. 17/159,347, 2021.
- Method and architecture for accelerating deterministic stochastic computing using residue number system, Mohammadhassan Najafi, Kamyar Givaki, Seyed Reza Hojabrossadati, MH Gholamrezayi, Ahmad Khonsari, Saeid Gorgin, Dara Rahmati
  US Patent App. 17/166,378, 2021.

Publications and manuals:

- M Daneshvaramoli, MS Kiarostami, SK Monfared, H karisani, A Visuri, S Hosio, D Rahmati, S Gorgin, " A Study on non-Overlapping Multi-Agent Pathfinding," Future of Information and Communication Conference (FICC), accepted, to be presented, March 2022.

- MS Karvandi, SK Monfared, MS Kiarostami, D Rahmati, S Gorgin, "A Way Around UMIP and Descriptor-Table Exiting via TSX-based Side-Channel," The 16th International Conference on Risks and Security of Internet and Systems (CRISIS), Iowa, USA, November 2021.

- S Kashi, A Patooghy, D Rahmati, M Fazeli, "An energy efficient synthesis flow for application specific SoC design," Elsevier Integration Journal, Vol 81, pp 331-341, 2021.

- SK Monfared, O Hajihassani, V Mohsseni, D Rahmati, S Gorgin, "A High-throughput Parallel Viterbi Algorithm via Bitslicing," ACM Transactions on Parallel Computing (TOPC) 8 (4), 1-25, 2021.

- Mohammad Sina Kiarostami, Mohammadreza Daneshvaramoli, Saleh Khalaj Monfared, Aku Visuri, Helia Karisani, Simo Hosio, Hamed Khashehchi, Ehsan Futuhi, Dara Rahmati, Saeid Gorgin, " On Using Monte-Carlo Tree Search to S.olve Puzzles," 7th International Conference on Computer Technology Applications, 2021.

- Mehdi Yousefzadeh, Parsa Esfahanian, Seyed Mohammad Sadegh Movahed, Saeid Gorgin, Dara Rahmati, Atefeh Abedini, Seyed Alireza Nadji, Sara Haseli, Mehrdad Bakhshayesh Karam, Arda Kiani, Meisam Hoseinyazdi, Jafar Roshandel, Reza Lashgari, " ai-corona: Radiologist-assistant deep learning framework for COVID-19 diagnosis in chest CT scans, "

- K Givaki, R Hojabr, MH Gholamrezaei, A Khonsari, S Gorgin, D Rahmati, M Hassan Najafi, "High Performance Deterministic Stochastic Computing Using Residue Number System," IEEE Design & Test Journal, 2021.

- M Baharloo, A Khonsari, M Dolati, P Shiri, M Ebrahimi, D Rahmati, "Traffic-aware performance optimization in Real-time wireless network on chip," Elsevier Nano Communication Networks Journal, Vol .26, 2020.

- A Ansari, M Asghari, S Gorgin, D Rahmati, "A Modified Grey Wolf Optimization for Energy Efficiency and Resource Wastage Balancing in Cloud Data-Centers," 10th International Conference on Computer and Knowledge Engineering," Mashhad, Iran, 2020.

- R Hojabr, K Givaki, K Pourahmadi, P Nooralinejad, A Khonsari, D Rahmati, M Hassan Najafi, "TaxoNN: A Light-Weight Accelerator for Deep Neural Network Training, " IEEE International Symposium on Circuits and Systems (ISCAS), 2020.

- SK Monfared, O Hajihassani, MS Kiarostami, SM Zanjani, D Rahmati, S Gorgin, "BSRNG: A High Throughput Parallel BitSliced Approach for Random Number Generators," 49th International Conference on Parallel Processing-ICPP: Workshops, Edmonton AB Canada, 2020.

- M Abbaszadeh, M Mazraeli, D Rahmati, SH Attarzadeh-Niaki, "ANDRESTA: An Automated NoC-Based Design Flow for Real-Time Streaming Applications," IEEE CSI/CPSSI International Symposium on Real-Time and Embedded Systems and Technologies (RTEST),Tehran, Iran, 2020.

- M Daneshvaramoli, MS Kiarostami, SK Monfared, H Karisani, K Dehghannayeri, D Rahmati, S Gorgin, "Decentralized Communication-less Multi-Agent Task Assignment with Cooperative Monte-Carlo Tree Search," 6th International Conference on Control, Automation and Robotics (ICCAR), 2020.

- K Givaki, B Salami, R Hojabr, SMR Tayaranian, A Khonsari, D Rahmati, S Gorgin, A Cristal, OS Unsal, "On the resilience of deep learning for reduced-voltage FPGAs," 28th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP), Västerås, Sweden, 2020.

- AH Hadian-Rasanan, D Rahmati, S Gorgin, K Parand, "A single layer fractional orthogonal neural network for solving various types of Lane–Emden equation," Elsevier New Astronomy Journal, Vol. 75, pp.101307, to be published Feb. 2020.

- M Daneshvaramoli, Mohammad Sina Kiarostami, Saleh Khalaj Monfared, Helia Karisani, Hamed Khashehchi, Dara Rahmati, Saeid Gorgin, Amir Rahmati, "Decentralized Cooperative Communication-less Multi-Agent Task Assignment with Monte-Carlo Tree Search," arXiv preprint arXiv:1910.12062, 2019.

- SK Monfared, O Hajihassani, SM Zanjani, S Kiarostami, D Rahmati, S Gorgin, "High-performance Cryptographically Secure Pseudo-random Number Generation via Bitslicing," arXiv preprint arXiv:1909.04750, 2019.

- MS Kiarostami, M Daneshvaramoli, SK Monfared, D Rahmati, S Gorgin, "Multi-Agent non-Overlapping Pathfinding with Monte-Carlo Tree Search," IEEE Conference on Games (CoG), 2019.

- K Givaki, R Hojabr, MH Najafi, A Khonsari, MH Gholamrezayi, S Gorgin, D Rahmati, "Using Residue Number Systems to Accelerate Deterministic Bit-stream Multiplication," IEEE 30th International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019

- R Hojabr, K Givaki, SM Tayaranian, P Esfahanian, A Khonsari, D Rahmati, "SkippyNN: An Embedded Stochastic-Computing Accelerator for Convolutional Neural Networks" Proceedings of the 56th Annual Design Automation Conference (DAC) 2019.

- D Rahmati, S Masoudi, A Khonsari and R Sabbaghi, “Accurate Performance Bounds Calculation for Dynamic Voltage-Frequency Islands in Best Effort Networks-on-Chip, ” 36th IEEE International Conference on Computer Design (ICCD), 2018.

- D Rahmati, H Sarbazi-Azad, “Classified Round Robin: A Simple Prioritized Arbitration to Equip Best Effort NoCs with Effective Hard QoS, ” IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE-TCAD), vol. 37, no. 1, 2018, pp. 257-269.

- S. Kashi, A. Patooghy, D. Rahmati, M. Fazeli and M. Kinsy, "Application Specific Networks-on-Chip Synthesis: An Energy Efficient Approach," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2018.

- M. Baharloo, A. Khonsari, P. Shiri, I. Namdari and D. Rahmati, "High-average and Guaranteed Performance for Wireless Networks-on-Chip Architectures," IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2018.

- O. Hajihassani, A. Ahmadzadeh, M. Gavahi, M. Raei, D. Rahmati and S. Gorgin, "A low-power hybrid non-volatile cache with asymmetric coding," 7th IEEE International Conference on Computer and Knowledge Engineering (ICCKE), Mashhad, 2017, pp. 277-282. (Best Paper Award)

- D Rahmati, S Murali, L Benini, F Angiolini, G De Micheli, H Sarbazi-Azad, "Computing Accurate Performance Bounds for Best Effort Networks-on-Chip," in IEEE Transactions on Computers (IEEE-TC), Vol. 62, No. 3, 2013, pp. 452-467.

- C Seiculescu, D Rahmati, S Murali, L Benini, G De Micheli and H Sarbazi-Azad, "Designing Best Effort Networks-on-Chip to Meet Hard Latency Constraints," In ACM Transactions on Embedded Computing Systems (ACM-TECS), Vol. 12, No. 4, Article 108, 2013.

- D Rahmati, H Sarbazi-Azad, S Hessabi, AE Kiasari, "Power-efficient deterministic and adaptive routing in torus networks-on-chip," in Elsevier Microprocessors and Microsystems Journal (MICPRO),Vol. 36, 2012, pp. 571-585.
- D Rahmati, S Murali, L Benini, F Angiolini, G De Micheli and H Sarbazi-Azad, "A method for calculating hard QoS guarantees for Networks-on-Chip," In Proceedings of International Conference on Computer Aided Design (ICCAD), 2009, pp. 579-586.
- D Rahmati, AE Kiasari, H Sarbazi-Azad and S Hessabi, "Power efficient routing algorithm for torus NoCs," In Proceedings of International Conference on Contemporary Computing (IC3), India, 2008, pp. 211–220.
- MA Tabar, S Koohi, D Rahmati, S Hessabi, “An Adaptive Approach to Manage the Number of Virtual Channels,” AINA 2008.
- AE Kiasari, D Rahmati, H Sarbazi-Azad and S Hessabi, "A Markovian Performance Model for Network-on-Chips," Proceeding of PDP 2008.
- MH Ghadiry, M Nadi, MT Manzuri-Shalmani, D Rahmati ,”The Effect of Number of Virtual Channel on NoC EDP,” ICCCE08.
- D Rahmati, AE Kiasari, S Hessabi, H Sarbazi-Azad, “A Performance and Power Analysis of WK-Recursive and Mesh Networks for Network-on-Chips,” International Conference on Computer Design (ICCD2006), 2006.
- M Nadi, MH Ghadiry, MT Manzuri-Shalmani , D Rahmati ,"Effect of Number of Faults on NoC Power and Performance," Proceeding of ICPADS 2007.
- D Rahmati, AS Zebardast, MH Reshadi, Z Navabi, “Handling Complex VHDL Semantics with an OO Intermediate Format,” Canadian Conference on Electrical and Computer Engineering, 2003.
- B Robatmili, H Ghasemi, D Rahmati, Z Navabi, “A Scalable Method for HDL Elaboration,” IST 2003.
- BH Yaran, D Rahmati and AS Zebardast, “Applying Cycle-Based Simulation Technique to VITAL as a VHDL Gate Level Standard,” Canadian Conference on Electrical and Computer Engineering, CCECE2001, May 2001.
- AS Zebardast, D Rahmati, BH Yaran, Z Navabi, “SP2V: Accelerating Post-layout SPICE Simulation using VERILOG Gate-level Modeling,“ Canadian Conference on Electrical and Computer Engineering, CCECE2001, May 2001.
- D Rahmati and AS Zebardast, “The Process of Error Recovery for Lex and Yacc standard,” Technical Report, CAD Lab, University of Tehran, December 1999.

Teaching Experiences:

- **VHDL Course** for undergraduate and graduate students
- **Verilog Course** for undergraduate and graduate students
- **Logic Circuit Course** for undergraduate students
- **Computer Architecture and Logic Circuits Lab**. for undergraduate students
- **Computer Architecture Course** for undergraduate students
- **Microprocessor and Microsystem Course** for undergraduate students
- **Embedded System Design Course** for undergraduate students
- **Digital System Test and Testable Design Course** for graduate students
- **Hardware Accelerator for Machine Learning Course** for graduate students
- **Research Method Course** for graduate students

Academic Reviewer:

- Reviewer for IEEE Transactions on Computers (TC)
- Reviewer for IEEE Transactions on Parallel and Distributed Systems (TPDS)
- Reviewer for IEEE Transactions on Computer Aided Design (TCAD)
- Reviewer for IET Computers & Digital Techniques Journal
- Reviewer for ACM Transactions on Design Automation of Electronic Systems (TODAES)
- Reviewer for Elsevier Computers & Electrical Engineering journal
- Reviewer for Elsevier Microprocessors and Microsystems journal

Awards and Honors:

- Ranked among the top 10th of about 200 undergraduates electrical and computer classmate students, September 1998.
- Ranked first in provincial undergraduate university entrance exams among more than 5000 participants, 1994.
- Awarded Bronze Medal at the Iranian Mathematics Olympiad, 1993.

Events organizing:

- **The workshop chair** of the **9th** IPM-HPC Workshop on Multi-core Systems and Graphic Processors, June, 2019.
  https://hpc.ipm.ac.ir/2019/06/08/9th-ipm-hpc-workshop-on-multi-core-systems-and-graphic-processors/
- **The workshop chair** of the **8th** IPM-HPC Workshop on Multi-core Systems and Parallel Platforms, March, 2019.
  https://hpc.ipm.ac.ir/2019/01/22/8th-ipm-hpc-workshop/
- **The workshop chair** of the **7th** IPM-HPC WorkShop on Multi-Core Systems & GPU and their applications in HPC, Feburary, 2018.
  https://hpc.ipm.ac.ir/2019/01/02/7th-ipm-hpc-workshop-on-multi-core-systems-gpu-and-its-application-in-hpc/

Expertise:

- Experienced in **Machine Learning**, using **High Performance Computing** resources (GPU/CPU Cluster) and **Open-MP/Cuda** programming tools used in Deep Learning, etc.
- Fully experienced in software programming languages such as **C++, C#, Python, Matlab, Basic, HTML, Perl, Linux Programming, Lex & Yacc compiler** design.
- Fully Experienced in many software programming environments including **Visual C++ .Net**, **Visual C# .Net**, **Borland C++ Builder**.
- Fully experienced in Hardware programming languages such as **VHDL, Verilog, Spice.**
- Familiar with many hardware programming environments, including ModelSim, Active VHDL, Leonardo Exemplar, MaxPlusII, Synplify, Synopsis FPGA Express, **Xilinx Vivado**, **Xilinx Foundation (ISE)**, HSPICE, Protel, LEDIT.
- Extensive experienc in **design and implementation** of **embedded systems, hardware, iot devices, electronics printable circuit board (PCB) design**, **test and prototyping**, including **FPGAs**, **Micro-controllers** and **communication circuitry**.
- Thorough understanding of hardware concepts, design, implementation and experienced at simulation techniques. Familiar and research on mathematical modeling techniques of computer architecture and Networks-on-Chip. Familiar with test generation and fault detection algorithms and VLSI design and synthesis process.
- Fully Experienced in object oriented and optimized data structure design and implementation.

Academic Experiences:

- Design the Real-Time Bound Extraction capability of Network-on-Chip for SUNFLOOR Platform, used for automatic synthesis of Networks-on-Chip, LSI Lab, EPFL University.
- Design and implementation of a platform for NoC VHDL modeling, synthesis and simulation, Sharif University of Technology.
- Design and Implementation of a Hybrid Interpreted-Compiled Code VHDL Event-Driven Simulator with Extensibility, as M.Sc. Thesis, University of Tehran.
- Implementation of a fully semantic-checking and also error-recovery portion of a full VHDL compiler and intermediate generation, University of Tehran.
- Working as a member of the CAD group in university of Tehran for the design and implementation of both a compiler and a simulator based on AIRE (Advanced Intermediate Representation with Extensibility / Common Environment) tool using MS visual C++.

- Layout generation of LUTBs and PALBs of an HFPA (Hybrid Field Programmable gate Array) with LEDIT software as Advanced VLSI course project.
- Design and implementation of a heterogeneous environment for parallel and remote java file compilation and execution as parallel processing course project.
- Design and Implementation of a 30 channel PC sound card using SSI ICs as B.Sc. thesis, May 1998, University of Tehran.

Keynotes:

- **Keynote speaker** at the First Regional **Conference on Smart Cities and Smart Electrical Networks**, titled: "**Low-Power Wide Area Networks (LPWAN) and Their IOT and Smart Grid Applications**", March 2018, Islamic Azad University, Saqqez, Iran.
- **Keynote speaker** at the First Advanced **workshop on IOT devices**, titled: "**Low Power Communication Protocols for Internet of Things and Cyber Physical Systems**", March 2019, University of Kurdistan, Sanandaj, Iran.

Industrial Experiences as Project Manager, Developer and also Consultant:

- **Product**: A Media Center system on Embedded systems using Linux OS on Raspberry Pi and Python programming, as Project Manager and Developer.
- **Product**: 4/8/64 (FXO-FXS) port VOIP IP-PBX switches with the softwares, as Project Manager and Developer.
- **Product**: Hardware Security Module (AKA Network Encryption Card), as Project Manager and Developer.
- **Product**: Wideband Electromagnetics Frequency Band Recorder and Player (with 80 MHz instantaneous bandwidth and several hours recording capacity), as consultant
- **Product**: GPS signal simulator, as consutant.
- **Products**: Several high speed FPGA and data acquisition boards, as Designer, Test engineer and Developer.
- **Service**: High speed and custom digital and analog Circuit design, test and production, as Designer and Developer.

Key Hardware and Electronics Courses Taken in Computer Engineering During my Undergraduate and Graduate Education:

- Advanced Computer Architecture
- Test and Testability of Digital Systems
- Design of Fault Tolerant Systems
- Hardware Description Language (VHDL)
- Verilog HDL
- VLSI Array Processors
- Advanced VLSI Circuit Design
- Interconnection Networks
- Advanced Computer Networks
- Digital Signal Processing
- Data Transmission
- Computer Interface Circuit Design
- Advanced Communication Systems
- Arithmetic Circuits
- Queuing Theory
- Fuzzy Systems
- Circuit Design (I,II)
- Digital Electronics (I,II)
- Microprocessors

Key Software Courses Taken in Computer Engineering during Undergraduate and Graduate Education:

- Computer Principles and Programming
- Advanced Computer Programming
- Data Structures
- Object Oriented System Design
- Operating System Design
- Data Storage and Retrieval
- Compiler Design

Other Courses:

- Stochastic Processes
- Queuing Theory
- Probability and Statistics
- Discrete Mathematics

Languages Proficiency:

- Kurdish (Native)
- Persian (Professional)
- English (Professional)
- French (Elementary)

Professional References:

Name: Amir Hossein Jahangir
Position: CEO of Shetab Saman Co., and Associate Professor, Computer Engineering Department, Sharif University of Technology
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Name: Hamid Sarbazi-azad
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Name: Ahmad Khonsari
Position: Associate Professor, ECE Department, University of Tehran
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Name: Ahmad Patooghy
Position: Assistant Professor, Department of Computer Systems Technology, North Carolina A&T State University of Central Arkansas, USA.
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