Mehdi Modarressi

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Date of birth: March 27, 1981

Nationality: Iranian

Martial status: married

Education

- Ph.D. in Computer Engineering, Sharif University of Technology, Tehran, Iran (2006-2011)
- M.Sc. in Computer Engineering, Sharif University of Technology, Tehran, Iran (2003-2005)
- B.Sc. in Computer Engineering, Amirkabir University of Technology (Tehran Polytechnic), Tehran, Iran (1999-2003)

Professional Experience

- Founder and Director, *Parallel and Network-based Processing Research Laboratory*, School of ECE, University of Tehran, Iran (2012-Now)
- Coordinator of the Students' Summer Internship Program, School of ECE, College of Engineering, University of Tehran (2016-Now)
- Non-resident Research Assistant, School of Computer Science, Institute for Studies in Fundamental Sciences (IPM), Tehran, Iran (2006-Now)

Research Visits and International Collaborations

- Coordinator an PI of the Erasmus+ Student/Staff mobility program between University of Tehran and Tallinn University of Technology (Estonia), (2022-2025)
- Project Co-director, *Energy-Efficient Hardware for Deep Learning-based Image Processing*, (funded by Stiftelsen för internationalisering av högre utbildning), Mälardalen University (MDU), Sweden, (Feb. 2019-Dec. 2019)
- Visiting Researcher (funded by DAAD), Technical University of Dresden, Germany (Jul. 2019-Sep. 2019)
- Visiting PhD student, PARSA Laboratory, École Polytechnique Fédérale de Lausanne (EPFL), Switzerland, (Dec. 2009-Sept. 2010)

Selected Talks/Presentations

- Hardware Architectures for Deep Learning, Invited talk, Technical University of Dresden, Germany, Aug. 2019.
- Hardware Architectures for Deep Learning, Invited talk, Tallinn University of Tech., Estonia, Apr. 2019.
- Hardware Architectures for Deep Learning, Invited talk, Malardalens University, Sweden, Mar. 2019.
- Low-power Parallel Data Processing Using Computation Reuse, ICICM conference, Moscow, Russia, 2017.
- Deep Learning at the Edge, IPM invited talk, Tehran, Iran, 2017.
- Low-Power Online ECG Analysis Using Neural Networks, DSD conference, Limassol, Cyprus, 2016.
- Fault-Tolerant 3-D NoC Design using Dynamic Link Sharing, DATE conference, Dresden, Germany, 2016.
- Hardware Accelerator for Protein Sequencing on NoCs, EWDTS conference, Batumi, Georgia, 2015
- Accelerating Memory Access in NoC-based CMPs, DATE conference, Grenoble, France, 2015.
- Reconfigurable NoC Architectures, IPM invited talk, Tehran, Iran, 2015.
- Game Theoretical Thermal- Aware Task Synchronization, DSD conference, Cesme, Turkey, 2012.
- Low-power arithmetic unit for DSP applications, SoC conference, Tampere, Finland, 2012.

Professional Service

- Track Chair, System and Hardware, Iran Informatics Conference, (2019-2023)
- Track Chair, Embedded Neuromorphic Computing Systems, 12th IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip, 2018.
- Guest Editor, Elsevier Journal of System Architecture, Special Issue on Networks-on-Chip, 2014.
- TPC Member:
  - Euromicro Conference on Parallel, Distributed, Network-based Computing (OCPNBS) (2013-2022)
  - IEEE International Symposium on Embedded Multicore/Many-core Systems-on-Chip (2016 -2022)
  - Euromicro Conference on Digital System Design (ASHWPA) (2018-2023)
  -ACM workshop on Many-core- Embedded Systems (2015-16)
  - IEEE Conference on Computer Architecture & Digital Systems (2013-2022)
  - Workshop on Hardware and Software Implementation and Control of Distributed MEMS (2010-2011)
  - International Conference on High Performance Computing & Simulation (2014-2016)
  - The CSI Symposium on Real-Time and Embedded Systems and Technologies (2015)
  - The CSI International Computer Conference (2012, 2013, 2016)
- Workshop organizer, *CloudSuite: a benchmark suite for cloud services*, in the CSI Computer Conference, Iran, 2012.
- Workshop organizer, *Embedded Deep Learning at the Edge*, University of Tehran, Iran, 2018-2022.
- Reviewer: IEEE CAL, IEEE TC, IEEE TCAS, IEEE TCAD, ACM Computing Surveys, Elsevier JSA, Elsevier Micpro, Elsevier CAEE, Elsevier JBE, Springer SUPE, DATE, ASP-DAC, ASAP, DSD, PDP, IPDPS, …

Courses

Since 2012, I teach the following courses every year at the Computer Engineering Section, School of ECE, University of Tehran:

- Graduate level:
  - ECE-489: Interconnection Networks (Fall semesters)
  - ECE-492: Chip Multiprocessors (Spring semesters)
- Undergraduate level:
  - ECE-381: Computer-Aided Design of Digital Systems (Fall semesters)
  - ECE-339: Real-Time Embedded Systems (Spring semesters)
  - ECE-301: Research Methods & Presentation Skills (Spring and Fall semesters)

I have taught these courses as guest lecturer in some semesters from 2007 to 2014:

- ECE-223: Microcontrollers (EE Section, school of ECE, University of Tehran)
- CE-411: Hardware Description Languages (Sharif University of Technology)
- CE-508: Hardware-Software Co-design (Sharif University of Technology)
- CE-422: VLSI (Sharif University of Technology)
- CE-361: Digital System Design (Sharif University of Technology)
- CE-452: Microprocessors (Sharif University of Technology

Projects and Grants

- 2022: University of Tehran-TalTech mobility Program, funded by Eramsum+, ~€10K
- 2021: Open Internet-of-Things Laboratory, funded by Iran National Science Foundation, ~€50K
- 2019: Grant for Research Stays for University Academics and Scientists, funded by German Academic Exchange Service (DAAD), €6K
- 2019: Energy-Efficient Hardware for Deep Learning-based Image Processing, funded by Stiftelsen för internationalisering av högre utbildning (STINT), 150K SEK (~€15k)
- 2016: FPGA board for real-time signal processing, funded by Ministry of Industry (co-PI), funded by Ministry of Industry, Mine and Trade of Iran, ~€20K
- 2014: Design and Manufacturing of Smart Phones and Tablets- a feasibility study (co-PI), funded by Ministry of Industry, Mine and Trade of Iran, ~€14K
- 2010: Mobility Grant for Outstanding PhD Students, Iran Telecommunication research center (now: CyberSpace Research Institute), ~€16K

Students Supervised

- PhD Alumni:
  - Arash Firuzan: Improving the resource utilization of many-core convolutional neural network accelerators using network-on-chip reconfiguration
  - Atefeh. S. Hosseini: Daylight adaptive smart indoor lighting system using neural networks
- Other alumni
  - 24 M.Sc. and 17 B.Sc. alumni
- Current students:
  - PhD: Sepideh Fattahi, Hossein A. Rezaei, Hoda Mahdiani, Bita Dabiri, Ardavan Elahi, Maryam Bahreinizad, Faraz Tahmasebi
  - MSc: Farugh Shayesteh-roodi, Sara Khodarahmi, Reyhaneh Hosseinzadeh, Sohrab Moradi

Publications

- One Book, 8 Book Chapters, 23 Journal papers, and 51 Conference papers (Publications in local journals and conferences are not listed)
  The scholar page for publications and citations: https://scholar.google.com/citations?user=z7UNzUoAAAAJ&hl=en

Book

1. M. Daneshtalab, M. Modarressi, Hardware Architectures for Deep Learning, IET publishers, UK, 2020. (IET link)(Amazon link)

Book Chapters

2. M. Sadrosadati, A. Mirhosseini, N. Akbarzadeh, M. Modarressi, H. Sarbazi-Azad, "Chapter 1: Traffic-load-aware virtual channel power-gating in network-on-chips", Advances in Computers (Power-Efficient Network-on-Chips: Design and Evaluation), Elsevier, Volume 124, 2022.
3. M. Modarressi, S. H. SeyyedAghaei Rezaei, "Chapter 7: Power-efficient network-on-chip design by partial topology reconfiguration", Advances in Computers (Power-Efficient Network-on-Chips: Design and Evaluation), Elsevier, Volume 124, 2022.
4. M. Modarressi, H Sarbazi-Azad, "Chapter 4: Topology Specialization for Networks-on-Chip in the Dark Silicon Era", Advances in Computers: Dark Silicon and Future of On-chip Systems, Elsevier, Volume 112, 2018.
5. M. Modarressi, H Sarbazi-Azad, "Chapter 1: A Reconfigurable On-Chip Interconnection Network for Large Multicore Systems", Large-scale Network-centric Distributed Systems, John Wiley & Sons, NJ, USA, 2014.
6. R. Jabbarvand, M. Modarressi, H. Sarbazi-Azad, "Chapter 4: Fault-Tolerant Routing Algorithms in Networks on-Chip", Routing Algorithms in Networks-on-Chip, Springer, 2014.
7. M. Modarressi, H Sarbazi-Azad, "Chapter 13: A High-Performance and Low-Power Reconfigurable Network-on-Chip Architecture", Dynamic Reconfigurable Network-on-Chip Design: Innovations for Computational Processing and Communication, IGI Global Pubs, 2010.
8. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, "Chapter 16: A novel de Bruijn based mesh topology for Networks-on-Chip", VLSI Design, IN-TECH Publishers, Austria, 2011. (ISBN 978-3-902613-50-9)
9. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, "Chapter 5: Shuffle-Exchange Mesh Topology for Networks-on-Chip", Parallel and Distributed Computing, IN-TECH Publishers, Austria, 2011. (ISBN: 978-3-902613-45-5)

Journal Papers

10. AR. Firuzan, M. Modarressi, M. Reshadi, A. Khademzadeh, "Reconfigurable Network-on-Chip based Convolutional Neural Network Accelerator", Elsevier Journal of Systems Architecture, 2022.
11. A. Ghanbari, M. Modarressi, "Energy-efficient acceleration of convolutional neural networks using computation reuse", Elsevier Journal of Systems Architecture, 2022.
12. A. Seyedolhosseini, M. Modarressi, N. Masoumi, N. Karimian, "Efficient photodetector placement for daylight-responsive smart indoor lighting control systems", Elsevier Journal of Building Engineering, 2021.
13. H. Mahdiani, A. Khadem, A. Ghanbari, M. Modarressi, F. Fattahi-Bayat and M. Daneshtalab, "ΔNN: Power-Efficient Neural Network Acceleration Using Differential Weights," IEEE Micro, 2020.
14. S. H. Seyyedaghaei Rezaei, M. Modarressi, R. Ausavarungnirun, M. Sadrosadati, O. Mutlu, M. Daneshtalab, "NOM: Network-on-Memory for Inter-Bank Data Transfer in Highly-Banked Memories", IEEE Computer Architecture Letters, 2020.
15. Seyedolhosseini, A., Masoumi, N., Modarressi, M. and Karimian, N., "Daylight adaptive smart indoor lighting control method using artificial neural networks", Elsevier Journal of Building Engineering, 2019.
16. M. Bakhshalipour, P. Lotfi-Kamran, A. Mazloumi, M. Naderan-Tahan, M. Modarressi, and H. Sarbazi-Azad, "Fast Data Delivery for Many-Core Processors," in IEEE Transactions on Computers, 2018.
17. M. Sadrosadati, A. Mirhosseini, M. Modarressi, H. Sarbazi-Azad, "BARAN: Bimodal Adaptive Reconfigurable-Allocator Network-on-Chip," ACM Transactions on Parallel Computing, 2018.
18. M. Keramati, M. Modarressi, and S. H. Seyedaghaei Rezaei. "Thermal management in 3d networks-on-chip using dynamic link sharing," Elsevier Microprocessors and Microsystems, 2017.
19. R. Hojabrossadati, M. Modarressi, A. Yasoubi, M. Daneshtalab, and A. Khounsari. "Customizing Clos Network-on-Chip for Neural Networks." IEEE Transactions on Computers, 2017.
20. A. Yasoubi, R. Hojabr, M. Modarressi, "Power-Efficient Accelerator Design for Neural Networks using Computation Reuse", IEEE Computer Architecture Letters, 2017.
21. P. Mehrvarzy, M. Modarressi, H Sarbazi-Azad, "Power- and performance-efficient cluster-based network-on-chip with reconfigurable topology", Elsevier Journal of Microprocessors and Microsystems, 2016.
22. P. Lotfi-kamran, M. Modarressi, H. Sarbazi-Azad, "An Efficient Hybrid-Switched Network-on-Chip for Chip Multiprocessors", IEEE Transactions on Computers, 2015.
23. S. H. Seyyedaghaei, A. Mazloumi, M. Modarressi, P. Lotfi-Kamran, "Dynamic Resource Sharing for High-Performance 3-D Networks-on-Chip", IEEE Computer Architecture Letters, 2016.
24. M. Modarressi, H. Sarbazi-Azad, "Leveraging Dark Silicon to Optimize Networks-on-Chip Topology", Springer Journal of Supercomputing, 2015.

25. F. Pakdamana, A. Mazloumia, M. Modarressi, "Integrated circuit-packet switching NoC with efficient circuit setup mechanism", Springer Journal of Supercomputing, 2015.
26. M. Modarressi, N. Teimouri, H. Sarbzai-Azad, "Improving the performance of packet-switched networks-on-chip by SDM-based adaptive shortcut paths", Elsevier Integration, the VLSI Journal, 2015.
27. M. Modarressi, M. Asadinia, H. Sarbazi-Azad, "Using Task Migration to Improve Non-contiguous Processor Allocation in NoC-based CMPs", Elsevier Journal of System Architecture, 2013.
28. M. Asadinia, M. Modarressi, H. Sarbazi-Azad, "New Non-contiguous Processor Allocation Algorithm in Mesh-based CMPs Using Virtual Point-to-point Links", IET Computers and Digital Techniques 2012.
29. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, "The 2D digraph-based NoCs: attractive alternatives to the 2D mesh NoCs", The Journal of Supercomputing, 2012.
30. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, "The 2D SEM: a novel high-performance and low-power mesh-based topology for networks-on-chip", International Journal of Parallel, Emergent, and Distributed Systems, 2010.
31. M. Modarressi, A. Tavakkol, H. Sarbazi-Azad, "Application-Aware Topology Reconfiguration for On-Chip Networks", IEEE Transactions on Very Large Scale Integrated Circuits, 2011.
32. M. Modarressi, A. Tavakkol, H. Sarbazi-Azad, "Virtual Point-to-Point Connections in NoCs", IEEE Transactions on Computer-Aided Design for Integrated Circuits and Systems, 2010.

Conference Papers

33. N. Neda, S. Ullah, A. Ghanbari, H. Mahdiani, M. Modarressi and A. Kumar, "Multi-Precision Deep Neural Network Acceleration on FPGAs," *27th Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2022.
34. B. Dabiri, M. Modarressi and M. Daneshtalab, "Network-on-ReRAM for Scalable Processing-in-Memory Architecture Design," *24th Euromicro Conference on Digital System Design (DSD)*, 2021.
35. V. Geraeinejad, S. Sinaei, M. Modarressi and M. Daneshtalab, "RoCo-NAS: Robust and Compact Neural Architecture Search," *International Joint Conference on Neural Networks (IJCNN)*, 2021
36. A. Firuzan, M. Modarressi, M. Daneshtalab, M. Reshadi, "Reconfigurable Network-on-Chip for 3D Neural Network Accelerators," IEEE/ACM International Symposium on Network-on-Chip (NOCS), Italy, 2018.
37. N. Akbari, M. Modarressi, M. Daneshtalab, M. Loni, "A Customized Processing-in-Memory Architecture for Biological Sequence Alignment," 29th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Italy, 2018.
38. A. Seyedolhosseini, N. Masoumi, M. Modarressi and N. Karimian, "Zone Based Control Methodology of Smart Indoor Lighting Systems Using Feedforward Neural Networks," *9th International Symposium on Telecommunications (IST)*, 2018
39. A. Seyedolhosseini, N. Masoumi, M. Modarressi and N. Karimian, "Design and Implementation of Efficient Smart Lighting Control System with Learning Capability for Dynamic Indoor Applications," *9th International Symposium on Telecommunications (IST)*, 2018
40. A. Seyedolhosseini, N. Masoumi, M. Modarressi and N. Karimian, "Illumination Control of Smart Indoor Lighting Systems Consists of Multiple Zones," *Smart Grid Conference (SGC)*, 2018,
41. P. Lotfi-Kamran, M. Modarressi, H. Sarbazi-Azad, "NOC Characteristics of Cloud Applications", The 19th International Symposium on Computer Architecture and Digital Systems (CADS), Iran, 2017. (Best Paper Award)
42. E. Momenzadeh, M. Modarressi, A. Mazloumi, and M. Dneshtalab "Parallel Forwarding for Efficient Bandwidth Utilization in Networks-on-Chip", 30th Conference on Architecture of Computing Systems (ARC), Austria, 2017.
43. N. Akbari, M. Modarressi. "A High-Performance Network-on-Chip Topology for Neuromorphic Architectures", 15th IEEE International Conference on Embedded and Ubiquitous Computing (EUC), China, 2017.
44. B. Dabiri, S. H. Seyedaghaei Rezaei, and M. Modarressi, "Low-power Parallel Data Processing Using Computation Reuse", 7th International Conference on Information Communication and Management, Russia, 2017.
45. A. Seyedolhosseini, N. Masoumi, and M. Modarressi, "Performance Improvement of ZigBee Networks in Coexistence of Wi-Fi Signals", 7th International Conference on Information Communication and Management, Russia, 2017.

46. P. Lotfi-Kamran, M. Modarressi, H. Sarbazi-Azad, “Near-Ideal Networks-on-Chip for Servers”, The 23rd IEEE Symposium on High Performance Computer Architecture (HPCA), USA, 2017.
47. M. Azimi, M. Modarressi, “Proactive Network-on-Chip Path Setup for Message Passing Programs”, Euromicro Conference on Digital System Design (DSD), Cyprus, 2016.
48. M. Modarressi, A. Yasoubi, Ma. Modarressi, “Low-Power Online ECG Analysis Using Neural Networks”, Euromicro Conference on Digital System Design (DSD), Cyprus, 2016.
49. A. Rezaei, M. Daneshtalab, D. Zhao, M. Modarressi, “SAMi: Self-Aware Migration Approach for Congestion Reduction in NoC-based MCSoC”, 29th IEEE International System-on-Chip Conference (SOCC), USA, 2016.
50. S. Sayardoost Tabrizi, I. Soltani Mohammadi, A. Mazloumi, M. Modarressi, “High Performance Hybrid-switched Network-on-Chip Using Shortcut Paths”, 24th Iranian Conference on Electrical Engineering (ICEE), Iran, 2016.
51. S. H. Seyyedaghaei Rezaei, M. Modarressi, S. Roshanisefat, M. Daneshtalab, “A Three-Dimensional Networks-on-Chip Architecture with Dynamic Buffer Sharing”, EuroMicro PDP Conference, Greece, 2016.
52. S. H. Seyyedaghaei Rezaei, M. Modarressi, R. Yazdani, M. Daneshtalab, “Fault-Tolerant 3-D Network-on-Chip Design using Dynamic Link Sharing”, the Conference on Design, Automation and Test in Europe (DATE'16), Germany, 2016.
53. M. Modarressi, F. Faghih, M. Modarressi, “Hardware Accelerator Protein Sequencing Applications on Reconfigurable Networks-on-Chip”, the 13th. East-West Design and Test Symposium (EWDTS), Georgia, 2015.
54. M. Faryabi, H. Dorosti, M. Modarressi and S. M. Fakhraei, “Process Variation-Aware Approximation for Efficient Timing Management of Digital Circuits”, the 13th. East-West Design and Test Symposium (EWDTS), Georgia, 2015.
55. A. Yasoubi, R. Hojabr, H. Takshi, M. Modarressi, M. Daneshtalab, “CuPAN-High Throughput On-chip Interconnection for Neural Networks”, International Conference of Neural Information Processing (ICONIP), 2015.
56. A Firuzan, M Modarressi, M Daneshtalab, “A Reconfigurable Network-on-Chip for Efficient Implementation of Neural Networks”, 10th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), Germany, 2015.
57. H. Mirhosseini, M. Sadrosadati, A. Fakhrzadehgany, M. Modarressi, and H. Sarbazi-Azad, “An Energy-Efficient Virtual Channel Power-Gating Mechanism for on-Chip Networks”, the Conference on Design, Automation and Test in Europe (DATE'15), France, 2015.
58. A. Mazloumi, M. Modarressi, “A Hybrid Packet/Circuit-switched Router to Accelerate Memory Access in NoC-based Chip Multiprocessors”, Design, Automation and Test in Europe (DATE'15), France, 2015.
59. M. Zaeemi, M. Modarressi, “An FPGA-Like Ultra Low-Power Network-On-Chip for Multicore Embedded Systems”, in the 11th. FPGAWORLD Conference, Denmark, 2014.
60. M. Modarressi, H. Sarbazi-Azad, “A Reconfigurable NoC Topology for the Dark Silicon Era”, the 11th. FPGAWORLD Conference, Denmark, 2014.
61. M. Modarressi, H. Sarbazi-Azad, “A reconfigurable network-on-chip architecture for heterogeneous CMPs in the dark-silicon era”, 25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'14), Switzerland, 2014.
62. N. Teimouri, M. Modarressi, H. Sarbazi-Azad, “Power and Performance-efficient Partial-circuits in Packet-switched Networks-on-Chip”, EuroMicro PDP, Ireland, 2013.
63. M. Modarressi, S.H. Nikounia, A. Jahangir, “Low-power arithmetic unit for DSP applications”, International Symposium on System on Chip (SoC), Finland, 2011.
64. M. Modarressi, H. Sarbazi-Azad, “Reconfigurable Cluster-based Networks-on-Chip for Application-specific MPSoCs”, 23rd IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP'12), Netherlands, 2012.
65. Y. Asgarieh, M. Khabbazian, M. Modarressi, H. Sarbazi-Azad, “A Game Theoretical Thermal - Aware Run - Time Task Synchronization Method for Multiprocessor Systems - on - Chip”, Euromicro Conference on Digital System Design (DSD), Turkey, 2012.
66. R. Jabbarvand, M. Modarressi, H. Sarbazi-Azad, “A Reconfigurable Fault-Tolerant Routing Algorithm to Optimize the Network-on-Chip Performance and Latency in Presence of Intermittent and Permanent Faults”, The 29th. International Conference on Computer Design (ICCD'11), USA, 2011.
67. M. Asadinai, M. Modarressi, A. Tavakkol, H. Sarbazi-Azad, “Supporting Non-contiguous Processor Allocation in CMPs Using Virtual Point-to-point Links”, Design Automation and Test in Europe Conference (DATE'11), France, 2011.

68. N. Teimouri, M. Modarressi, H. Sarbazi-Azad: Energy-Optimized On-Chip Networks Using Reconfigurable Shortcut Paths, the 23rd. Conference of Architectures for Computing Systems (ARCS'11), Italy, 2011.
69. M. Modarressi, H. Sarbazi-Azad, A. Tavakkol, "An Efficient Dynamically Reconfigurable On-chip Network Architecture", Design Automation conferecne (DAC'10), USA, 2010.
70. M. Asefi, M. Modarressi, H. Sarbazi-Azad, "A Load-balanced Routing Scheme for NoCs", Workshop on MEMS (DMEMS'10), France, 2010.
71. S. Sahhaf, M. Modarressi, H. Sarbazi-Azad, "A Novel SDM-based On-chip Communication Mechanism", The Fourth European Conference of Modern Information and Communication Technologies (ECUMICT'10), Belgium, 2010.
72. M. Modarressi, H. Sarbazi-Azad, A. Tavakkol, "Low-power and High-Performance On-Chip Communication Using Virtual Point-to-Point Connections", The IEEE/ACM International Symposium on Network-on-Chip (NoCS'09), USA, 2009.
73. M. Modarressi, H. Sarbazi-Azad, M. Arjomand, "An SDM-Based Hybrid Packet-Circuit-Switched On-Chip Network", Design, Automation, and Test in Europe Conference (DATE'09), France, Apr.2009.
74. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, " The 2D DBM: An Attractive Alternative to the Simple 2D Mesh Topology for On-Chip Networks", the 26th. International Conference on Computer Design (ICCD'08), USA, 2008.
75. R. Sabbaghi, M. Modarressi, H. Sarbazi-Azad, "A Novel High-Performance and Low-Power Mesh-Based NoC", the 7th. IPDPS Workshop on Performance Modeling, Evaluation, and Optimization of Ubiquitous Computing and Networked Systems (IPDPS'08 PMEO), USA, 2008.
76. M. Modarressi, H. Sarbazi-Azad, "Virtual Point-to-Point Links in Packet-Switched NoCs", IEEE International Symposium on VLSI (ISVLSI), 2008.
77. M. Modarressi, H. Sarbazi-Azad, "Power-Aware Mapping for Reconfigurable NoC Architectures", The 25th. International Conference on Computer Design (ICCD'07), USA, 2007.
78. S. Hessabi, M. Modarressi, M. Goudarzi, H. Javan-Hemmat, "A Table-Based Application-Specific Prefetch Engine for Object-Oriented Embedded Systems", International Conference on Embedded Computing Systems: Architectures, Modeling, and Simulation (IC-SAMOS VI), Greece, 2006.
79. M. Modarressi, S. Hessabi, M. Goudarzi, "A Reconfigurable Cache Architecture for Object-Oriented Application-Specific Processors", Canadian Conference on Electrical and Computer Engineering (CCECE'06), Canada, 2006.
80. M. Modarressi, H. Javan-Hemmat, S.G. Miremadi, S. Hessabi, M. Najafvand, M. Goudarzi, M. Mohamadzadeh, "A Fault-Tolerant Approach to Embedded-System Design Using Software Standby Sparing", The 11th. International CSI Computer Conference (CSICC'06), Iran, 2006.
81. M. Modarressi, S. Hessabi, M. Goudarzi, "A Data Prefetching Mechanism for Object-Oriented Embedded Systems Using Run-Time Profiling", The Third IEEE Symposium on Electronic Design, Test, and Applications (DELTA'06), Malaysia, 2006.
82. M. Modarresi, H. Sarbazi-Azad, "Parallel 3-Dimensional DCT Computation on k-Ary n-Cubes ", The 8th International Conference on High Performance Computing in Asia Pacific Region (HPC-Asia 2005), China, 2005.
83. M. Modarressi, M. Goudarzi, S. Hessabi: Application-Specific Hardware-Driven Prefetching to Improve Data Cache Performance. Asia-Pacific Computer Systems Architecture Conference (ACSAC'05) Singapore, 2005.

Other

84. M. Daneshtalab, P. Liljeberg, M. Modarressi, and L. Soreas, Editorial, Special issue on network-based many-core embedded systems, Elsevier Journal of System Architecture, 2013.
85. M. Modarressi, "High-performance and Low-power Reconfigurable NoC Topology", DATE'09 PhD Forum, France, 2009.
86. M. Modarressi, "An Efficient Dynamically Reconfigurable On-chip Network Architecture", ACM Student Research Competition at PACT (ACM SRC), Austria, 2010. (Silver Medal