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CURRENT POSITIONS:

- **Professor**, School of Electrical and Computer Engineering, University of Tehran, August 1995-present.
 - **Director**, Low-Power High-Performance Nanosystems Laboratory, School of Electrical and Computer Engineering, University of Tehran, 2005-present.
 - **Director**, Silicon Intelligence Laboratory, School of Electrical and Computer Engineering, University of Tehran, 2015-present.

EDUCATION:

- **Ph.D. Electrical Engineering**, University of Michigan, Ann-Arbor, U.S.A., Sept. 1991-Aug. 1994.
- **M.Sc. Electrical Engineering**, University of Pittsburgh, Pittsburgh, U.S.A., Jan. 1990-April 1991.
- **B.Sc. Electrical Engineering**, Sharif University of Technology, Tehran, Iran, Feb. 1984-Feb. 1988.

RESEARCH AREAS OF INTERESTS/EXPERIENCES:

- ❖ Low-Power High-Performance Circuits/Architectures/Systems.
- ❖ Nano-electronics.
- ❖ Optoelectronic Devices.

PROFESSIONAL SERVICES:

- International Journals
 - **Associate Editor**: ACM Journal of ACM Transactions on Design Automation of Electronic Systems, February 2009 – December 2012.
- International Conferences
 - **Technical Program Committee Member**: IEEE ISQED: Since 2007.
 - **Technical Program Committee Member**: IEEE ASQED: Since 2009–2015.
 - **Technical Program Committee Member**: IEEE DTIS: 2006–2010 and 2012–2018.
 - **Technical Program Committee Member**: IEEE ISVLSI: 2011.
 - **Technical Program Committee Member**: IEEE GLSVLSI: 2007 – 2008.
 - **Technical Program Committee Member**: Student (Ph.D.) Forum of IEEE ASP-DAC: 2006–2008.
 - **Technical Program Committee Member**: Interdisciplinary Engineering Design Education Conference (IEDEC): 2012–2014.

PROFESSIONAL EXPERIENCES:

- **Research Fellow**, VLSI group, Department of Electrical and Computer Engineering, University of Waterloo, Jan. 1999-Aug. 1999.
Investigated substrate coupling in Mixed-Signal IC's.
- **Research Fellow**, VRG, Department of Electrical and Computer Engineering, University of Toronto, Sept. 1998-Dec. 1998.
Investigated RF power MOSFET design, modeling and fabrication.
- **Research Fellow**, Center for Display Technology & Manufacturing, EECS Dept., University of Michigan, 1994-1995.
Investigated field-emission microelectronic devices for flat panel display applications.
Developed Finite Element Programs for Modeling Field Emitters.

PREVIOUS UNIVERSITY ADMINISTRATIVE SERVICES:

- **Vice Dean of Engineering for Undergraduate and Graduate Studies**, College of Engineering, University of Tehran, Jan. 2010-May 2015.
- **Director**, Nanoelectronics Center of Excellence, University of Tehran, 2005-2007.
- **Head**, Electronics Division, School of Electrical and Computer Engineering, University of Tehran, 2005-2007.
- **Member**, IT Committee, School of Electrical and Computer Engineering, 2003-2006.
- **Member**, University Informatics Policy Making Committee, 2000- 2003.
- **Head**, Engineering Division, Center for E-Learning, 2002-2003.
- **Head**, Informatics Center, College of Engineering, 1999-2002.
- **Head**, Computer Center, School of Electrical and Computer Engineering, 1999-2001.

PUBLICATIONS

BOOK CHAPTER:

1. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Ultra-low Power Implementation of Neural Networks Using Inverter-based Memristive Crossbars" in *Book Chapter Contribution Invitation: Electronic Design for AI, IoT and Hardware Security*, Springer, 2023.
2. A. Fayyazi, M. Ansari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Inverter-Based Memristive Neuromorphic Circuit for Ultra-Low-Power IoT Smart Applications," in *Hardware Architectures for Deep Learning*, M. Daneshtalab and M. Modaressi, IET, 2020.
3. M. Hemmat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Robust Hybrid TFET-MOSFET Circuits in Presence of Process Variations and Soft Errors" in T. Hollstein, J. Raik, S. Kostin, A. Tšertov, I. O'Connor, R. Reis (eds.) *VLSI-SoC: System-on-Chip in the Nanoscale Era – Design, Verification and Reliability*, VLSI-SoC 2016. IFIP Advances in Information and Communication Technology, vol. 508. Springer, Cham, DOI:10.1007/978-3-319-67104-8_3, 2017.
4. X. Zhang, **A. Afzali-Kushaa**, T.B. Norris, G.I. Haddad, and J.P. Sung "Investigations Towards Far-Infrared (THz) Lasers Based on Quantum Wells" in *Long Wavelength Infrared Emitters Based on Quantum Wells and Superlattices*, Gordon & Beach Publishers, 1999.

JOURNALS:

1. F. Ebrahimi-Azandaryani, O. Akbari, M. Kamal, **A. Afzali-Kusha**, M. Pedram, "Accuracy Configurable Adders with Negligible Delay Overhead in Exact Operating Mode," in *ACM Transactions on Design Automation of Electronic Systems*, vol. 28, no. 1, pp 1–14, [doi: 10.1145/3549936](https://doi.org/10.1145/3549936).
2. S. Taghipour, M. Kamal, R. Niaraki-Asli, A. Afzali-Kusha and M. Pedram, "LCHC-DFT: A Low-Cost High-Coverage Design-for-Testability Technique to Detect Hard-to-Detect Faults in STT-MRAMs in the Presence of Process Variations," in *IEEE Transactions on Device and Materials Reliability*, vol. 22, no. 4, pp. 477-487, Dec. 2022, [doi: 10.1109/TDMR.2022.3201754](https://doi.org/10.1109/TDMR.2022.3201754).
3. M. Ahmadzadeh, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "A2P-MANN: Adaptive Attention Inference Hops Pruned Memory-Augmented Neural Networks," Accepted for publication in *IEEE Transactions on Neural Networks and Learning Systems*, January 26, 2022.
4. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Loading-Aware Reliability Improvement of Ultra-Low Power Memristive Neural Networks," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 8, pp. 3411-3421, Aug. 2021.
5. M-A Maleki, A-R Nabipour-Meybodi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "An Energy-Efficient Inference Method in Convolutional Neural Networks Based on Dynamic Adjustment of the Pruning Level," in *ACM Transactions on Design Automation of Electronic Systems*, vol. 26, no. 6, Nov. 2021, pp 1–20.

6. M. Soltani, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "An Adaptive Memory Side Encryption Method for Improving Security and Lifetime of PCM-based Main Memory," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, DOI: [10.1109/TCAD.2021.3093832](https://doi.org/10.1109/TCAD.2021.3093832).
7. S. Taghipour, M. Kamal, R. Niaraki-Asli, **A. Afzali-Kusha**, and M. Pedram, "CD-DFT: A Current-Difference Design-for-Testability to Detect Short Defects of STT-MRAM Under Process Variations," in *IEEE Transactions on Device and Materials Reliability*, vol. 21, no. 3, pp. 436-443, Sept. 2021.
8. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Reliability Enhancement of Inverter-Based Memristor Crossbar Neural Networks Using Mathematical Analysis of Circuit Non-Idealities," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 10, pp. 4310-4323, Oct. 2021.
9. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "LATIM: Loading-Aware Offline Training Method for Inverter-Based Memristive Neural Networks," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 10, pp. 3346-3350, Oct. 2021.
10. E. Tanghatari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Distributing DNN training over IoT edge devices based on transfer learning, in *Neurocomputing*, vol. 467, 2022, pp. 56-65.
11. R. Yarmand, M. Kamal, **A. Afzali-Kusha**, M. Pedram, "OPTIMA: An Approach for Online Management of Cache Approximation Levels in Approximate Processing Systems," in *IEEE Transactions on Very Large-Scale Integration Systems (TVLSI)*, vol. 29, no. 2, pp. 434-446, Feb. 2021.
12. S. Amanollahi, M. Kamal, **A. Afzali-Kusha**, M. Pedram, "Circuit-Level Techniques for Logic and Memory Blocks in Approximate Computing Systems," *Proceedings of the IEEE*, vol. 108, no. 12, pp. 2150-2177, 2020.
13. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "INTERSTICE: Inverter-Based Memristive Neural Networks Discretization for Function Approximation Applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 7, pp. 1578-1588, July 2020.
14. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Offline Training Improvement of Inverter-based Memristive Neural Networks Using Inverter Voltage Characteristic Smoothing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, doi: 10.1109/TCSII.2020.2997384.
15. P. Haghi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "O⁴-DNN: A Hybrid DSP-LUT-Based Processing Unit With Operation Packing and Out-of-Order Execution for Efficient Realization of Convolutional Neural Networks on FPGA Devices," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3056-3069, September 2020, doi: 10.1109/TCSI.2020.2986350.
16. O. Akbari, M. Kamal, **A. Afzali-Kusha**, M. Shafique, and M. Pedram, "X-CGRA: An Energy-Efficient Approximate Coarse-Grained Reconfigurable Architecture," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 10, pp. 2558-2571, Oct. 2020.
17. N. Samimi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Res-DNN: A Residue Number System-Based DNN Accelerator Unit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 2, pp. 658-671, Feb. 2020.
18. E. Bank-Tavakoli, S.A. Ghasemzadeh, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "POLAR: A Pipelined/Overlapped FPGA-Based LSTM Accelerator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 3, pp. 838-842, March 2020.

19. M. Soltani, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "RandShift: An Energy-Efficient Fault-Tolerant Method in Secure Nonvolatile Main Memory," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 1, pp. 287-291, Jan. 2020.
20. R. Yarmand, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "DART: A Framework for Determining Approximation Levels in an Approximable Memory Hierarchy," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 1, pp. 273-286, Jan. 2020.
21. F. Ebrahimi-Azandaryani, O. Akbari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Block-Based Carry Speculative Approximate Adder for Energy-Efficient Applications," *IEEE Transactions on Circuits and Systems II (TCAS-II)*, vol. 67, no.1, pp. 1371-141, 2020.
22. M. Ansari, A. Fayyazi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "OCTAN: An On-Chip Training Algorithm for Memristive Neuromorphic Circuits," *IEEE Transactions on Circuits and Systems I (TCAS-I)*, vol. 66, no. 12, pp. 4687-4698, 2019.
23. S.S. Nabavi-Larimi, M. Kamal, and **A. Afzali-Kusha**, "BIMS: Built-in Intermediate Memory Structure to Improve Multi-Level Phase Change Memories," *Tabriz Journal of Electrical Engineering*, vol. 49, no. 3, pp. 1405-1414, Fall 2019.
24. G. Pasandi, K. Mehrabi, B. Ebrahimi, S.M. Fakhraei, **A. Afzali-Kusha**, and M. Pedram, "Low-power data encoding/decoding for energy-efficient static random access memory design," in *IET Circuits, Devices & Systems*, vol. 13, no. 8, pp. 1152-1159, 2019.
25. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "TOSAM An Energy Efficient Truncation and Rounding Based Scalable Approximate Multiplier," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 1161-1173, 2019.
26. S. Sayyah-Ensan, M.H. Moaiyeri, B. Ebrahimi, S. Hessabi, and **A. Afzali-Kusha**, "A low-leakage and high-writable SRAM cell with back-gate biasing in FinFET technology," *Journal of Computational Electronics*, vol. 18, pp. 519–526, March, 2019.
27. M. Pashaeefar, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 327-340, 2019.
28. S. Tabatabaei-Nikkhah, M. Zahedi, M. Kamal, **A. Afzali-Kusha**, M. Pedram, "ACHILLES: Accuracy-Aware High-Level Synthesis Considering Online Quality Management," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 8, pp. 1465-1173, 2018.
29. O. Akbari, M. Kamal, **A. Afzali-Kusha**, M. Pedram, and M. Shafique, "Towards Approximate Computing for Coarse-Grained Reconfigurable Architectures," *IEEE Micro*, vol. 38, no. 6, pp. 63-72, 2018.
30. M. Pashaeefar, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications," *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 26, no. 11, pp. 2530-2541, 2018.
31. A. Fayyazi, M. Ansari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "An Ultra Low-Power Memristive Neuromorphic Circuit for Internet of Things Smart Sensors", *IEEE Internet of Things Journal*, vol. 5, no. 2, pp. 1011-1022, 2018.

32. S. Abolmali, M. Kamal, **A. Afzali-Kusha**, and M. Pedram “An Efficient False Path-Aware Heuristic Critical Path Selection Method with High Process Space Coverage,” *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, vol. 23, no. 3, pp. 32:1-32:25, 2018.
33. F. Nakhaee, M. Kamal, **A. Afzali-Kusha**, M. Pedram, S. M. Fakhraie, and H. Dorosti, “Lifetime Improvement by Exploiting Aggressive Voltage Scaling during Runtime of Error-resilient Applications,” *Integration, the VLSI Journal*, vol. 61, pp. 29-38, March 2018.
34. A. Iranfar, M. Kamal, **A. Afzali-Kusha**, M. Pedram, and D. Atienza, “TheSPoT: Thermal Stress-Aware Power and Temperature Management for Multiprocessor Systems-on-Chip,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 8, pp. 1532-1545, 2018.
35. M. Ansari, A. Fayyazi, A. Banagozar, M. A. Maleki, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “PHAX: Physical Characteristics Aware Ex-Situ Training Framework for Inverter-Based Memristive Neuromorphic Circuits,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 8, pp. 1602-1613, 2018.
36. O. Akbari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “RAP-CLA: A Reconfigurable Approximate Carry Look-Ahead Adder,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 8, pp. 1089-1093, Aug. 2018.
37. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “LETAM: A Low Energy Truncation-based Approximate Multiplier,” *Computers and Electrical Engineering*, vol. 63C, pp. 1-17, October 2017.
38. S. Abolmali, N. Mansouri-Ghiasi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “Efficient Critical Path Identification based on Viability Analysis Method Considering Process Variations,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 25, no. 9, September 2017, pp. 2668-2672.
39. O. Akbari, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “Dual-Quality 4:2 Compressors for Utilizing in Dynamic Accuracy Configurable Multipliers,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 25, no. 4, April 2017, pp. 1352-1361.
40. R. Zendegani, M. Kamal, M. Bahadori, **A. Afzali-Kusha**, and M. Pedram, “RoBA Multiplier: A Rounding-Based Approximate Multiplier for High-Speed yet Energy-Efficient Digital Signal Processing,” *IEEE Transactions on Very Large Scale Integration Systems (TVLSI)*, vol. 25, February 2017, pp. 393–401, DOI: 10.1109/TVLSI.2016.2587696.
41. M. Bahadori, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “An Energy and Area Efficient yet High-Speed Square-Root Carry Select Adder Structure,” *Computers and Electrical Engineering*, vol. 58, February 2017, pp. 101–112.
42. M. Hemmat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, “Hybrid TFET-MOSFET Circuit: A Solution to Design Soft-Error Resilient Ultra-Low Power Digital Circuit,” *Integration, the VLSI Journal*, vol. 57, January 2017, pp. 11–19.
43. M. Bahadori, M. Kamal, **A. Afzali-Kusha**, Y. Afsharnezhad, and E. Zahraie Salehi “CL-CPA: A Hybrid Carry-Lookahead/Carry-Propagate Adder for Low-Power or High-Performance Operation Mode,” *Integration, the VLSI Journal*, vol. 57, January 2017, pp. 62–68.
44. K. Mehrabi, B. Ebrahimi, R. Yarmand, **A. Afzali-Kusha**, and H. Mahmoodi, “Read static noise margin aging model considering SBD and BTI effects for FinFET SRAMs,” *Microelectronics Reliability*, vol. 65, October 2016, pp. 20–26.

45. M. Hemmat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Study On the Impact of Device Parameter Variations on Performance of III-V Homo Junction and Heterojunction Tunnel FETs," *Solid-State Electronics*, vol. 124, October 2016, pp. 46–53.
46. H. Ahmadi-Balef, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "All-Region Statistical Model for Delay Variation based on Log-Skew-Normal Distribution," *IEEE Transactions on Computer-Aided Design*, vol. 35, September 2016, pp. 1503–1508.
47. M. Bahadori, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "A Comparative Study on Performance and Reliability of 32-bit Binary Adders," *Integration, the VLSI Journal*, vol. 53, March 2016, pp. 54–67.
48. M. Kamal, Q. Xie, M. Pedram, **A. Afzali-Kusha**, and S. Safari "An Efficient Temperature Dependent Hot Carrier Injection Reliability Simulation Flow," *Microelectronics Reliability*, vol. 57, February 2016, pp. 10–19.
49. M. Bahadori, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "High-Speed and Energy-Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 2, February 2016, pp. 421–433.
50. M. Kamal, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "Yield and Speedup Improvements in Extensible Processors by Allocating Extra Cycles to Some Custom Instructions," *ACM Transactions on Design and Automation of Electronics Systems (TODAES)*, vol. 21, January 2016, pp. 28:1–28:25.
51. N. Jafarzadeh, M. Palesi, S. Eskandari, S. Hessabi, and **A. Afzali-Kusha**, "Low Energy yet Reliable Data Communication Scheme for Networks on Chip," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, DOI: 10.1109/TCAD.2015.2440311, vol. 34, no. 12, December 2015, pp. 1892 – 1904.
52. B. Ebrahimi, R. Asadpour, **A. Afzali-Kusha**, and M. Pedram, "A FinFET SRAM cell design with BTI robustness at high supply voltages and high yield at low supply voltages," *International Journal of Circuit Theory and Applications*, vol. 43, no. 12, pp. 2011–2024, December 2015, DOI: 10.1002/cta.2057.
53. M. Nejat, B. Alizadeh, and **A. Afzali-Kusha**, "Dynamic Flip-Flop Conversion: A Time-Borrowing Method for Performance," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, DOI:10.1109/TVLSI.2014.2366918, vol. 23, no. 11, November 2015, pp. 2724–2727.
54. N. Ghobadi and **A. Afzali-Kusha**, "Investigation and modeling of negative bias temperature instability (NBTI) and hot carrier injection (HCI) in nanometer multi-gate devices," *Iranian Journal of Electrical and Electronics Engineering*, vol. 12, no. 2, Fall 2015, pp. 1–14 (in Persian).
55. M. Kamal, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "OPLE: A Heuristic Custom Instruction Selection Algorithm Based on Partitioning and Local Exploration," *ACM Transactions on Embedded Computing Systems (TECS)*, vol. 14, no. 4, September 2015, Article No. 72.
56. B. Eghbalkhah, M. Kamal, H. Afzali-Kusha, **A. Afzali-Kusha**, M. B. Ghaznavi-Ghouschi, and M. Pedram, "Workload and Temperature Dependent Evaluation of BTI-Induced Lifetime Degradation in Digital Circuits," *Microelectronics Reliability*, vol. 55, issue 8, July 2015, pp. 1152–1162.
57. V. Akhlaghi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "An Efficient Network on-Chip Architecture Based on Isolating Local and non-Local Communications," *Computers & Electrical Engineering*, Available online 19

- December 2014, doi:10.1016/j.compeleceng.2014.12.002. vol. 45, July 2015, pp. 430-444.
58. M. Ansari, H. Afzali-Kusha, B. Ebrahimi, Z. Navabi, **A. Afzali-Kusha**, and M. Pedram, "A Near-Threshold 7T SRAM Cell with High Write and Read Margins and Low Write Time for Sub-20 nm FinFET Technologies," *Integration, the VLSI Journal*, vol. 50, June 2015, pp. 91–106.
 59. M. Nickray and **A. Afzali-Kusha**, "Simultaneous Power Control and Power Management algorithm with Sector-shaped Topology for Wireless Sensor Networks," *EURASIP Journal on Wireless Communication and Networking*, April 2015, 2015:118, doi:10.1186/s13638-015-0355-9.
 60. M. Kamal, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "Design of NBTI-Resilient Extensible Processors," *The VLSI Journal of Integration*, vol. 49, March 2015, pp. 22–34, <http://dx.doi.org/10.1016/j.vlsi.2014.12.001>.
 61. H.-R. Ahmadi, **A. Afzali-Kusha**, M. Pedram, and M. Mosaffa, "A Flexible, Prime-Field, Genus 2 Hyperelliptic-Curve Cryptography Processor with Low Power Consumption and Uniform Power Draw," *Electronics and Telecommunications Research Institute (ETRI)*, vol. 37, no. 1, February 2015, pp. 107–117, <http://dx.doi.org/10.4218/etrij.15.0114.0418>.
 62. B. Eghbalkhah, M. Kamal, **A. Afzali-Kusha**, M. B. Ghaznavi-Ghouschi, and M. Pedram, "CSAM: A Clock Skew-aware Aging Mitigation Technique," *Microelectronics Reliability*, vol. 55, issue 1, January 2015, pp. 282–290.
 63. B. Ebrahimi, **A. Afzali-Kusha**, and H. Mahmoodi, "Robust FinFET SRAM design based on dynamic back-gate voltage adjustment," *Microelectronics Reliability*, vol. 54, issue 11, November 2014, pp. 2604–2612.
 64. A. Yazdanbakhsh, M. Kamal, S.M. Fakhraie, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "Implementation-aware selection of the custom instruction set for extensible processors," *Microprocessors and Microsystems*, vol. 38, issue 7, October 2014, pp. 681–691.
 65. M. Kamal, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "Impact of Process-Variations on Speedup and Maximum Achievable Frequency of Extensible Processors," *ACM Journal of Emerging Technologies*, vol. 10, issue 3, April 2014, article no. 19.
 66. N. Jafarzadeh, M. Palesi, A. Khademzadeh, and **A. Afzali-Kusha**, "Data Encoding Techniques for Reducing Energy Consumption in Networks on Chip," in *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 22, no. 3, March 2014, pp. 675-685.
 67. M. Kamal, A. Yazdanbakhsh, H. Noori, **A. Afzali-Kusha**, and M. Pedram, "A New Merit Function for Custom Instruction Selection under an Area Budget Constraint," *Design Automation for Embedded Systems*, September 2013, DOI 10.1007/s10617-013-9117-2, vol. 17, Issue 1, pp 1-25.
 68. M. Kamal, **A. Afzali-Kusha**, S. Safari, and M. Pedram, "Considering the Effect of Process Variations during the ISA Extension Design Flow," *Microprocessors and Microsystems*, vol. 37, no. 6-7, August–October 2013, pp. 713–724.
 69. B. Afzal, B. Ebrahimi, **A. Afzali-Kusha**, and H. Mahmoodi, "An analytical model for read static noise margin including soft oxide breakdown, negative and positive bias temperature instabilities," *Microelectronics Reliability*, vol. 53, no. 5, May 2013, pp. 670-675.
 70. B. Afzal, B. Ebrahimi, **A. Afzali-Kusha**, and H. Mahmoodi, "Modeling read SNM considering both soft oxide breakdown and negative bias temperature

- instability,” *Microelectronics Reliability*, vol. 52, no. 12, December 2012, pp. 2948-2954.
71. B. Afzal, **A. Afzali-Kusha**, and M. Pedram, “Analytical Modeling of Read Margin Probability Distribution Function of SRAM Cells in Presence of Process Variations and NBTI Effect,” *Japanese Journal of Applied Physics*, vol. 51, no. 11, November 2012, 114301–1:9.
 72. H. Aghababa, B. Ebrahimi, **A. Afzali-Kusha**, and M. Pedram, “Probability calculation of read failures in nano-scaled SRAM cells under process variations,” *Microelectronics Reliability*, vol. 52, no. 11, November 2012, pp. 2805-2811.
 73. S. Mohammadi, **A. Afzali-Kusha**, and S. Mohammadi, “Performance Improvement of Partially Silicon-on-Insulator Lateral Double-Diffused Metal Oxide Semiconductor Field Effect Transistors Using Doping-Engineered Drift Region,” *Japanese Journal of Applied Physics*, vol. 51, no. 10, October 2012, pp. 101201–1:6.
 74. H. Aghababa, A. Khosropour, **A. Afzali-Kusha**, B. Forouzandeh, and M. Pedram, “Statistical Estimation of Leakage Power Dissipation in Nano-Scale CMOS Digital Circuits using Generalized Extreme Value Distribution,” *IET Circuits, Devices & Systems*, vol. 6, no. 5, September 2012, pp. 273-278.
 75. B. Afzal, B. Ebrahimi, **A. Afzali-Kusha**, and S. Mohammadi “Calculation of on-state I–V characteristics of LDMOSFETs based on an accurate LDD resistance modeling,” *Superlattices and Microstructures*, vol. 52, no. 3, September 2012, pp. 560–576.
 76. G. Rostami, M. Shahabadi, **A. Afzali Kusha**, and A. Rostami, “Nanoscale all-optical plasmonic switching using electromagnetically induced transparency,” *Applied Optics*, vol. 51, no. 21, July 2012, pp. 5019-5027.
 77. M. Tinati, A. Khademzadeh, **A. Afzali-Kusha**, M. Janidarmian, “HACS: A novel cost aware paradigm promising fault tolerance on mesh-based network on chip architecture,” *Computers & Electrical Engineering*, vol. 38, no. 4, July 2012, pp. 963-974.
 78. M. Saremi, **A. Afzali-Kusha**, and S. Mohammadi, “Ground plane fin-shaped field effect transistor (GP-FinFET): A FinFET for low leakage power circuits,” *Microelectronic Engineering*, vol. 95, July 2012, pp. 74-82.
 79. H. Aghababa, B. Forouzandeh, and **A. Afzali-Kusha**, “High-performance low-leakage regions of nano-scaled CMOS digital gates under variations of threshold voltage and mobility,” *Journal of Zhejiang University - Science C*, vol. 13, no. 6, June 2012, pp. 460-471.
 80. M. Nickray, **A. Afzali-Kusha**, and R. Jäntti, “MEA: an energy efficient algorithm for dense sector-based wireless sensor networks,” *EURASIP Journal on Wireless Communication and Networking*, no. 85, March 2012, pp. 1-13.
 81. B. Ebrahimi, B. Afzal, **A. Afzali-Kusha**, and S. Mohammadi “A RESURF LDMOSFET with a dummy gate on partial SOI,” *Journal of the Korean Physical Society*, vol. 60, no. 5, March 2012, pp. 842-848.
 82. M. Daneshtalab, M. Kamali, M. Ebrahimi, S. Mohammadi, **A. Afzali-Kusha**, and J. Plosila, “Adaptive Input-Output Selection Based On-Chip Router Architecture,” *Journal of Low Power Electronics*, vol. 8, no. 1, February 2012, pp. 11-29.
 83. G. Rostami, M. Shahabadi, **A. Afzali-Kusha**, and A. Rostami, “EIT based tunable metal composite spherical nanoparticles,” *Photonics and Nanostructures – Fundamentals and Applications*, vol. 10, no. 1, January 2012, 102–111.

84. B. Afzal, B. Ebrahimi, **A. Afzali-Kusha**, and M. Pedram, "An accurate analytical I-V model for sub-90-nm MOSFETs and its application to read SNM modeling," *Journal of Zhejiang University-SCIENCE C (Computer & Electronics)*, vol. 13, no. 1, January 2012, pp. 58-70.
85. M. Saremi, B. Ebrahimi, **A. Afzali-Kusha**, and S. Mohammadi "A partial-SOI LDMOSFET with triangular buried-oxide for breakdown voltage improvement" *Microelectronics Reliability*, vol. 51, no. 12, December 2011, pp. 2069-2076.
86. S. Mohammadi, **A. Afzali-Kusha**, and S. Mohammadi, "Drain current model for strained-Si/Si_{1-x}Ge_x/strained-Si double-gate MOSFETs including quantum effects," *Semiconductor Science and Technology*, vol. 26, no. 9, September 2011, 095022 doi: 10.1088/0268-1242/26/9/095022.
87. H. Aghababa, R. Asadpour, **A. Afzali-Kusha**, and B. Forouzandeh "Finding optimum value of numerical aperture for the best aerial image quality," *IEICE Electronics Express*, December 2011, vol. 8, no. 11, pp. 879-883.
88. M. Rostami, B. Ebrahimi, **A. Afzali-Kusha**, and M. Pedram, "Statistical Design Optimization of FinFET SRAM Using Back-Gate Voltage" *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 19, no. 10, October 2011, pp. 1911-1916.
89. M. E. Salehi, M. Samadi, M. Najibi, **A. Afzali-Kusha**, M. Pedram, S. M. Fakhraie, "Dynamic Voltage and Frequency Scheduling for Embedded Processors Considering Power and Timing Constraints" *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 19, no. 10, October 2011, pp. 1931-1935.
90. P. Lotfi-Kamran, A.-M. Rahmani, A.-A. Salehpour, **A. Afzali-Kusha**, and Z. Navabi, "Dynamic Power Reduction of Stalls in Pipeline Architecture Processors," *International Journal of Design, Analysis and Tools for Integrated Circuits and Systems*, vol. 1, no. 1, pp. 9-15, June 2011.
91. S. Mohammadi, **A. Afzali-Kusha**, and S. Mohammadi, "Compact Modeling of Short Channel Effects in Symmetric and Asymmetric 3-T/4-T Double Gate MOSFETs" *Microelectronics Reliability*, vol. 51, no. 3, March. 2011, pp. 543-549.
92. H.-R. Ahmadi, **A. Afzali-Kusha**, and M. Pedram "A power-optimized low-energy elliptic-curve crypto-processor" *IEICE Electronics Express*, December 2010, vol. 7, no. 23, pp. 1752-1759.
93. H.-R. Ahmadi and **A. Afzali-Kusha**, "A Low-Power and Low-Energy Flexible GF(p) ECC Processor," *Journal of Zhejiang University-SCIENCE C (Computer & Electronics)*, vol. 11, no. 9, 2010, pp. 724-736.
94. P. Lotfi-Kamran, A.-M. Rahmani, M. Daneshtalab, **A. Afzali-Kusha**, and Z. Navabi, "EDXY-A Smart Congestion-Aware and Link Failure Tolerant Routing Algorithm for Network-on-Chips," *Journal of Systems Architecture*, vol. 56, no. 7, 2010, pp. 256-264.
95. E. Rokhsat-Yazdi, **A. Afzali-Kusha**, and M. Pedram, "A High-Efficiency, Auto Mode-Hop, Variable-Voltage, Ripple Control Buck Converter," *Journal of Power Electronics*, vol. 10, no. 2, March 2010, pp. 115-124.
96. S. Mohammadi and **A. Afzali-Kusha**, "Modeling of drain current, capacitance and transconductance in thin film undoped symmetric DG MOSFETs including quantum effects," *Microelectronics Reliability*, vol. 50, no. 3, March 2010, pp. 338-345.
97. S. Mohammadi and **A. Afzali-Kusha**, "An Efficient Quantum-Based Model for the Threshold Voltage of Thin Film Double Gate/Silicon on Insulator Silicon Metal

- Oxide Semiconductor Field Effect Transistors,” *Japanese Journal of Applied Physics*, vol. 49, no. 2, February 2010, pp. 024304-1:8.
98. A.-M. Rahmani, **A. Afzali-Kusha**, and M. Pedram, “A Novel Synthetic Traffic Pattern for Power/Performance Analysis of Network-on-Chips Using Negative Exponential Distribution,” *Journal of Low Power Electronics*, vol. 5, no. 3, October 2009, pp. 396-405.
 99. A.-M. Rahmani, M. Daneshtalab, **A. Afzali-Kusha**, and M. Pedram, “Forecasting-Based Dynamic Virtual Channel Management for Power Reduction in Network-on-Chips,” *Journal of Low Power Electronics*, vol. 5, no. 3, October 2009, pp. 385-395.
 100. G. Razavipour, **A. Afzali-Kusha**, and M. Pedram, “Design and Analysis of Two Low Power SRAM Cell Structures,” *IEEE Transactions on Very Large Scale Integrated Circuits*, vol. 17, no. 10, Oct. 2009, pp. 1551 – 1555.
 101. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, “Sign Bit Reduction Encoding For Low Power Applications,” *Journal of VLSI Signal Processing Systems*, September 2009, vol. 57, no. 3, pp. 321 – 329.
 102. M. Daneshtalab, M. Ebrahimi, S. Mohammadi, and **A. Afzali-Kusha**, “Low-distance Path-based Multicast Routing Algorithm for Network-on-Chips,” *IET Proceedings of Computer and Digital Techniques*, vol. 3, no. 5, pp. 430-442, Sept. 2009.
 103. M. Saneei, **A. Afzali-Kusha**, and M. Pedram, “Two High Performance and Low Power Serial Communication Interfaces for On-chip Interconnects,” *Canadian Journal of Electrical and Computer Engineering*, Winter/Spring 2009, vol. 34, no 1/2. pp. 49 – 56.
 104. M. Mottaghi-Dastjerdi, **A. Afzali-Kusha**, and M. Pedram, “BZ-FAD: A Low-Power Low-Area Multiplier based on Shift-and-Add Architecture,” *IEEE Transactions on Very Large Scale Integrated Circuits*, 2009, vol. 17, no. 2, pp. 302 – 306.
 105. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, “A Low-Power High Throughput Link Splitting Router for NoCs,” *Journal of Zhejiang University-SCIENCE A*, 2008, vol. 9, no. 12, pp. 1708 – 1714.
 106. M. Samadi and **A. Afzali-Kusha**, “Dynamic power management with fuzzy decision support system,” *IEICE Electronics Express*, August 2008, vol. 5, no. 19, pp. 789 – 795.
 107. A. Abbasian, S. Hatami, **A. Afzali-Kusha**, and M. Pedram, "Wavelet-Based Dynamic Power Management for Non-stationary Service Requests," *ACM Transactions on Design Automation of Electronic Systems*, 2008, vol. 13, no. 1, article 13, pp. 13:1-13:41.
 108. H. Parezdeh-Afshar, M. Saneei, **A. Afzali-Kusha**, and M. Pedram, "Fast INC-XOR codec for low-power address buses," *IET Proceedings of Computer and Digital Techniques*, 2007, vol. 1, no. 5, pp. 625-631.
 109. A. Mehran, S. Saeidi, A. Khademzadeh, and **A. Afzali-Kusha**, "Spiral: A heuristic mapping algorithm for network on chip," *IEICE Electronics Express*, 2007, vol. 4, no. 15, August 10, 2007, pp. 478-484.
 110. F. Aezinia and **A. Afzali-Kusha**, "Low Power High Performance Level Converter for Dual Supply Voltage Systems," *IEICE Electronics Express*, vol. 4 (2007), no. 9, pp. 306-311.
 111. A. Amirabadi, **A. Afzali-Kusha**, Y. Mortazavi, and M. Nourani, “Clock Delayed Domino Logic with Efficient Variable Threshold Voltage Keeper,” *IEEE*

- Transaction on Very Large Scale Integrated Circuits*, vol. 15, no. 2, February 2007, pp. 125-134.
112. S. Sharifi, J. Jaffari, M. Hosseinabady, **A. Afzali-Kusha**, and Z. Navabi, "Scan-Based Structure with Reduced Static and Dynamic Power Consumption," to appear in *Journal of Low Power Electronics*, vol. 2, no. 3, Dec. 2006, pp. 477-487.
 113. **A. Afzali-Kusha**, M. Nagata, N.K. Verghese, and D.J. Allstot, "Substrate Noise Coupling in SoC Design: Modeling, Avoidance, and Validation," *Proceedings of the IEEE*, vol. 94, no. 12, Dec. 2006, pp. 2109-2138.
 114. K. Shoaee, M. Gholipour, **A. Afzali-Kusha**, and M. Nourani, "Comparative study of asynchronous pipeline design methods", *IEICE Electronics Express*, vol. 3, no. 8, April 2006, pp. 163-171.
 115. B. Bornoosh, **A. Afzali-Kusha**, R. Dehghani, M. Mehrara, S.M. Atarodi, and M. Nourani, "Reduced Complexity 1-Bit High-Order Digital Delta-Sigma Modulator for Low-Voltage Fractional-N Frequency Synthesis Applications," *The IEE-Proceedings Circuits, Devices & Systems*, vol. 152, no. 5, October 2005, pp. 471-477.
 116. P. Hashemi, A. Behnam, E. Fathi, **A. Afzali-Kusha**, and M. El Nokali, "2-D Modeling of Potential Distribution and Threshold Voltage of Short Channel Fully Depleted Dual Material Gate SOI MESFET," *Solid-State Electronics*, vol. 49, no. 8, pp. 1341-1346, August, 2005.
 117. B. Afzal, A. Zahabi, A. Amirabadi, Y. Koolivand, **A. Afzali-Kusha**, and M. El Nokali, "Analytical Model for C-V Characteristic of Fully-Depleted SOI-MOS Capacitors," *Solid-State Electronics*, vol. 49, no. 8, pp. 1262-1273, August, 2005.
 118. M. Maddah, H. Soltanian-Zadeh, **A. Afzali-Kusha**, A. Shahrokni, Z.G. Zhange, "Three-Dimensional Analysis of Complex Branching Vessels in Confocal Microscopy Images," *Computerized Medical Imaging and Graphics*, vol. 29, pp. 487-498, no. 6, 2005.
 119. S.H. Rasouli, A. Khademzadeh, **A. Afzali-Kusha**, and M. Nourani "Low-power single and double edge-triggered flip-flops for high speed applications," *IEE Proceedings-Circuits, Devices and Systems*, vol. 152, no. 2, pp. 118-122, April 2005.
 120. B. Hekmatshoar, S. Mohajerzadeh, D. Shahrjerdi, **A. Afzali-Kusha**, M.D. Robertson, and A. Tonita, "Low-temperature copper-induced lateral growth of polycrystalline germanium assisted by external compressive stress," *Journal of Applied Physics*, vol. 97, issue 4, Feb., 2005, pp. 044901-1-5.
 121. D. Shahrjerdi, B. Hekmatshoar, A. Khakifirooz, and **A. Afzali-Kusha**, "Optimization of the V_T -Control Method for Low-Power Ultra-Thin Double-Gate SOI Logic Circuits," *The VLSI Journal of Integration*, vol. 38, issue 3, January 2005, pp. 505-513.
 122. S. Hatami, M.Y. Azizi, H.R. Bahrami, D. Motavalizadeh, and **A. Afzali-Kusha** "Accurate and Efficient Modeling of SOI MOSFET with Technology Independent Neural Networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 11, pp. 1580-1587, 2004.
 123. A. Abbasian, S.H. Rasouli, A. Afzali-Kusha, and M. Nourani "No-race Charge Recycling Complementary Pass transistor Logic (NCRCL) and its Pipeline Event-driven Structure for Low Power Applications," *IEE Proceedings of Computer and Digital Techniques*, vol. 151, no. 3, pp. 183-190, May 2004.

124. S. Bolouki, M. Maddah, A. Afzali-Kusha, and M. El Nokali, "A Unified I-V model for PD/FD SOI MOSFETs with a Compact Model for Floating Body Effects," *Solid-State Electronics*, vol. 47, no. 11, pp. 1909-1915, November 2003.
125. T. Maleki, S. Mohajerzadeh, and **A. Afzali-Kusha**, "Plastic Micromachining Assisted by Ultra-violet Illumination," *IEEE Transactions on Electron Devices*, vol. 50, no. 8, pp. 1813-1815, August 2003.
126. M. Maddah, H. Soltanian-Zadeh, and **A. Afzali-Kusha**, "Snake Modeling and Distance Transform to Vascular Centerline Extraction and Quantification," *Computerized Medical Imaging and Graphics*, vol. 27, no. 6, pp. 503-512, April 2003.
127. M. Maddah, **A. Afzali-Kusha**, and H. Soltanian-Zadeh, "Efficient centerline extraction for quantification of vessels in confocal microscopy images," *Med. Phys.*, vol. 30, no. 2, pp. 203-211, February, 2003.
128. H. Mahmoodi-Meimand, **A. Afzali-Kusha** and M. Nourani, "Adiabatic carry look-ahead adder with efficient power clock generator," *IEE Proceedings-Circuits, Devices and Systems*, vol. 148, no. 5, pp. 229-234, 2001.
129. S. M.-J. Okhovat-Alavian, **A. Afzali-Kusha**, and M. Kamarei, "Intersubband relaxation in conduction band quantum wells," Winter Edition, *Amir-Kabir University Journal of Engineering*, vol. 12, no. 45, pp. 53-62, 2001. (in Persian).
130. C.Y. Sung, T.B. Norris, **A. Afzali-Kushaa**, and G.I. Haddad, "Femtosecond Intersubband Relaxation and Population Inversion in Stepped Quantum Wells," *Applied Physics Letters*, vol. 68, no. 4, pp. 435-437, 1996.
131. **A. Afzali-Kushaa** and G.I. Haddad, "Effects of Biaxial Strain on the Intervalence-band Absorption Spectra of InGaAs/InP Systems," *Journal of Applied Physics*, vol. 77, no. 12, pp. 6549-6 556, 1995.
132. **A. Afzali-Kushaa** and G.I. Haddad, "High Frequency Characteristics of MESFET's," *Solid State Electronics*, vol. 38, no. 2, pp. 401-406, Feb. 1995.
133. X. Zhang, **A. Afzali-Kushaa**, W.L. Chen, G. Munns, and G.I. Haddad, "Absorption and Population Inversion in p-type InGaAs Strained Layers Based on Intervalence Subband Transitions at FIR Frequencies," *Infrared Phys. Technol.* vol. 36, no. 1, pp. 545-550, 1995.
134. **A. Afzali-Kushaa**, G.I. Haddad, and T.B. Norris, "Optically Pumped Intersubband Lasers Based on Quantum Wells," *IEEE Journal of Quantum Electronics*, vol. 31, no. 1, pp. 135-143, Jan. 1995.
135. **A. Afzali-Kushaa** and G.I. Haddad, "Efficient Calculation of the Scattering Rates in Valence Band Quantum Wells," *Physical Review B (Condensed Matter)*, vol. 50, no. 11, pp. 7701-7; 15 Sept. 1994.
136. **A. Afzali-Kushaa** and M. El-Nokali, "Modeling the MOS Transistor," *International Journal of Electronics*, vol. 74, no. 2, pp. 213-229, 1993.
137. **A. Afzali-Kushaa** and M. El-Nokali, "Modeling Subthreshold Capacitances of MOS Transistors," *Solid State Electronics*, vol. 35, no. 1, pp. 45-49, Jan. 1992.

CONFERENCES/SYMPOSIUMS:

1. A. BanaGozar, S.H. Hashemi-Shadmehri, S. Stuijk, M. Kamal, **A. Afzali-Kusha**, and H. Corporaal, "ReMeCo: Reliable Memristor-Based in-Memory Neuromorphic Computation," in *Proceedings of the 28th Asia and South Pacific Design Automation Conference*, ASPDAC '23: January 2023, pp. 396–401, doi: [10.1145/3566097.3567889](https://doi.org/10.1145/3566097.3567889).
2. S.H. Hashemi-Shadmehri, A. BanaGozar, S. Stuijk, M. Kamal, **A. Afzali-Kusha**, Massoud Pedram, and H. Corporaal, "SySCIM: SystemC-AMS Simulation of Memristive Computation In-Memory," in *Proceedings of 2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Antwerp, Belgium, 2022, pp. 1467-1472, doi: [10.23919/DATE54114.2022.9774749](https://doi.org/10.23919/DATE54114.2022.9774749).
3. M. Vaeztourshizi, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "An Energy-Efficient, Yet Highly-Accurate, Approximate Non-Iterative Divider," in *the Proceedings of International Symposium on Low Power Electronics and Design (ISLPED)*, Seattle, USA, Article no. 14, July 23-25, 2018
4. O. Akbari, M. Kamal, **A. Afzali-Kusha**, M. Pedram, M. Shafique, "PX-CGRA: Polymorphic Approximate Coarse-Grained Reconfigurable Architecture," in *the Proceedings of Design Automation and Test in Europe (DATE)*, Dresden, Germany, March 19-23, 2018.
5. S. Vahdat, M. Kamal, **A. Afzali-Kusha**, M. Pedram, Z. Navabi, "TruncApp: A Truncation-based Approximate Divider for Energy Efficient DSP Applications," in *the Proceedings of Design Automation and Test in Europe (DATE)*, Lausanne, Switzerland, pp. 1635-1638, March 2017.
6. A. BanaGozar, M. A. Maleki, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Robust neuromorphic computing in the presence of process variation," in *the Proceedings of Design Automation and Test in Europe (DATE)*, Lausanne, Switzerland, pp. 440-445, March 2017.
7. M. Hemmat, M. Kamal, **A. Afzali-Kusha**, and M. Pedram, "Hybrid TFET-MOSFET Circuits: An Approach to Design Reliable Ultra-Low Power Circuits in the Presence of Process Variation," in *the Proceedings of IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Tallinn, Estonia, September 26-28, 2016, DOI: [10.1109/VLSI-SoC.2016.7753578](https://doi.org/10.1109/VLSI-SoC.2016.7753578).
8. S.S. Nabavi-Larimi, M. Kamal, **A. Afzali-Kusha**, and H. Mahmoodi, "Power and Energy Reduction of Racetrack-based Caches by Exploiting Shared Shift Operations," in *the Proceedings of IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Tallinn, Estonia, September 26-28, 2016, DOI: [10.1109/VLSI-SoC.2016.7753563](https://doi.org/10.1109/VLSI-SoC.2016.7753563).
9. R. Zendegani, M. Kamal, **A. Afzali-Kusha**, and Massoud Pedram, "SEERAD: A High Speed yet Energy-Efficient Rounding-based Approximate Divider", in *the Proceedings of Design Automation and Test in Europe (DATE)*, Dresden, Germany, pp. 1481-1484, March 14-18, 2016.
10. K. Mehrabi, B. Ebrahimi and **A. Afzali-Kusha**, "A Robust and Low Power 7T SRAM Cell Design," in *Proceedings of 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS)*, Tehran, Iran, pp. 1-6, Oct. 7-8, 2015, doi: [10.1109/CADS.2015.7377782](https://doi.org/10.1109/CADS.2015.7377782).
11. A. Iranfar, S. Nazar-Shahsavani, M. Kamal, and **A. Afzali-Kusha**, "A Heuristic Machine Learning-based Algorithm for Power and Thermal Management of Heterogeneous MPSoCs," in *Proceedings of International Symposium on Low*

- Power Electronics and Design (ISLPED)*, Rome, Italy, pp. 291 - 296, July 22-24, 2015, DOI: 10.1109/ISLPED.2015.7273529.
12. M. Kamal, A. Iranfar, **A. Afzali-Kusha**, and M. Pedram, "A thermal stress-aware algorithm for power and temperature management of MPSoCs," in *Proceedings of Design Automation and Test in Europe (DATE)*, Grenoble, France, pp. 954-959, March 9-13, 2015, DOI: 10.7873/DATE.2015.0761.
 13. R. Yarmand, B. Ebrahimi, H. Afzali-Kusha, **A. Afzali-Kusha**, and M. Pedram, "High Performance and High Yield 5 nm Underlapped FinFET SRAM Design Using P type Access Transistors," in *Proceedings of International Symposium on Quality Electronic Design*, March 2-4, 2015.
 14. B. Bozorgzadeh, S. Shahdoost, and **A. Afzali-Kusha**, "Delay variation analysis in the presence of power supply noise in nano-scale digital VLSI circuits," in *Proceedings of International Midwest Symposium on Circuits and Systems (MWSCAS)*, College Station, Texas, August 3-6, 2014, pp. 117-120.
 15. M. Nejat, B. Alizadeh, and **A. Afzali-Kusha**, "Dynamic Flip-Flop conversion to tolerate process variation in low power circuits," in *Proceedings of Design Automation and Test in Europe (DATE)*, DOI: 10.7873/DATE.2014.124, March 24-28, 2014.
 16. M. Kamal, A. Ghasemazar, **A. Afzali-Kusha**, and M. Pedram, "Improving Efficiency of Extensible Processors by Using Approximate Custom Instructions," in *Proceedings of Design Automation and Test in Europe (DATE) Conference*, DOI: 10.7873/DATE.2014.238, March 24-28, 2014.
 17. A. Ghasemazar, M. Goli, and **A. Afzali-Kusha**, "Embedded Complex Floating Point Hardware Accelerator," in *Proceedings of International Conference on VLSI Design*, DOI: 10.1109/VLSID.2014.61, Mumbai, India, January 5-9, 2014, pp. 318 – 323.
 18. M. Y. Zarei, R. Asadpour, S. Mohammadi, **A. Afzali-Kusha**, R. Seyyedi, "Modeling symmetrical independent gate FinFET using predictive technology model" in *Proceedings of Great Lakes Symposium on VLSI (GLSVLSI)*, Paris, France, May 2-4, 2013, pp. 299-304.
 19. B. Eghbalkhah, S. A. Kashani-Gharavi, **A. Afzali-Kusha**, and M. B. Ghaznavi-Ghouschi, "Self-impact of NBTI effect on the degradation rate of threshold voltage in PMOS transistors," in *Proceedings of Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Abu Dhabi, UAE, March 26-28, 2013, pp. 151-154.
 20. M. Kamal, **A. Afzali-Kusha**, S. Safari, M. Pedram, B. Eghbalkhah, "Capturing and mitigating the NBTI effect during the design flow for extensible processors," in *Proceedings of Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Abu Dhabi, UAE, March 26-28, 2013, pp. 94-97.
 21. B. Ebrahimi, **A. Afzali-Kusha**, N. Sehatbakhsh, "Robust polysilicon gate FinFET SRAM design using dynamic back-gate bias," in *Proceedings of Design & Technology of Integrated Systems in Nanoscale Era (DTIS)*, Abu Dhabi, UAE, March 26-28, 2013, pp. 171 – 172.
 22. V. Akhlaghi, M. Kamal, **A. Afzali-Kusha**, M. Pedram, "An efficient network on-chip architecture based on isolating local and non-local communications," *Proceedings of the Design, Automation and Test in Europe*, March 18-22, Grenoble, France, 2013, pp. 350-353.
 23. M. Kamal, Q. Xie, M. Pedram, **A. Afzali-Kusha** and S. Safari, "An Efficient Reliability Simulation Flow for Evaluating the Hot Carrier Injection Effect in

- CMOS VLSI Circuits,” in *Proceedings of IEEE International Conference on Computer Design*, Montreal, Canada, Sept. 30 – Oct. 3, 2012, pp. 352 – 357.
24. B. Ebrahimi and **A. Afzali-Kusha**, “Analysis of SRAM Cell Characteristics Based on High-k Metal-Gate Strained Si/Si_{1-x}Ge_x MOSFET with Consideration of NBTI/PBTI,” in *Proceedings of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, Seville, Spain, September 19 – 21, 2012, pp. 137 – 140.
 25. B. Ebrahimi, H. Afzali-Kusha, and **A. Afzali-Kusha**, “Low Power and Robust 8T/10T Subthreshold SRAM Cells,” in *Proceedings of International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design*, Seville, Spain, September 19 – 21, 2012, pp. 141 – 144.
 26. M. Saffari, S. Lotfi, N. Jafarzadeh, and A. Afzali-Kusha, “Mapping of cores on to diagonal mesh-based network-on-chip,” in *Proceedings of Mediterranean Conference on Embedded Computing (MECO)*, Bar, Montenegro, June 19–21, 2012, pp. 233 – 238.
 27. A. Khosropour, S.-A. Kashani-Gharavi, Reza Asadpour, and **A. Afzali-Kusha**, “Process Variation Tolerant SRAM Cell Design Using Additive Model Considering NBTI Effect,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Penang, Malaysia, July 10 – 11, 2012, pp. 46 - 53.
 28. B. Ebrahimi, R. Asadpour, and **A. Afzali-Kusha**, “Low-Power and Robust SRAM Cells Based on Asymmetric FinFET Structures,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Penang, Malaysia, July 10 – 11, 2012, pp. 41 - 45.
 29. S. Soleimani-Amiri, **A. Afzali-Kusha**, and A. Sammak, “Design and analysis of a new sub-threshold DT MOS SRAM cell structure,” in *Proceedings of International Symposium on Computer Architecture and Digital Systems (CADS)*, Shiraz, Iran, May 2-3, 2012, pp. 50-53.
 30. M. Kamal, S. Safari, **A. Afzali-Kusha**, and M. Pedram, “An Architecture-Level Approach for Mitigating the Impact of Process Variations on Extensible Processors,” in *Proceedings of the Design, Automation and Test in Europe*, Dresden, Germany, March 12-16, 2012, pp. 1-4.
 31. A. Khosropour, H. Aghababa, B. Forouzandeh, and **A. Afzali-Kusha**, “Chip Level Statistical Leakage Power Estimation Using Generalized Extreme Value Distribution” in *Proceedings of the International Workshop on Power and Timing Modeling Optimization and Simulation (PATMOS)*, Madrid, Spain, September 26-29, 2011, pp. 173-179.
 32. A. Alimardani, M. Noei, E. Asl-Soleimani, and **A. Afzali-Kusha**, “Simulation and Optimization of CIGS Solar Cells in Concentrated Sunlight,” in *Proceedings of the ISES Solar World Congress*, Kassel, Germany, 28 August - 2 September, 2011, pp. 1-7.
 33. A. Alimardani, E. Asl-Soleimani, and **A. Afzali-Kusha**, “Simulation and Optimization of Emitter Depth and Doping for Silicon Solar Cells under Concentrated Sunlight,” in *Proceedings of the ISES Solar World Congress*, Kassel, Germany, 28 August - 2 September, 2011, pp. 1-7.
 34. A. Alimardani, N. Manavizadeh, **A. Afzali-Kusha**, and E. Asl-Soleimani, “Simulation of lateral effect in emitter region of silicon solar cells for concentrated sunlight,” in *Proceedings of the 12th Int. Conf. on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, (EuroSimE), Linz, Austria, April 18-20, 2011, art. no. 5765820, pp. 1-5.

35. M. Kamal, **A. Afzali-Kusha**, and M. Pedram “Timing Variation-Aware Custom Instruction Extension Technique,” in *Proceedings of the Design, Automation and Test in Europe*, March 14-18, Grenoble, France, 2011, pp. 1- 4.
36. M. Saremi, B. Ebrahimi, and **A. Afzali-Kusha**, “Ground Plane SOI MOSFET Based SRAM With Consideration of Process Variation,” in *Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits*, Hong Kong, December 15-17, 2010, pp. 1-4.
37. S.-N. Mozaffari, H. Aghababa, and **A. Afzali-Kusha**, “Joint-PDF of Timing and Power of Nano-scaled CMOS Digital Gates due to Channel Length Variation,” in *Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits*, Hong Kong, December 15-17, 2010, pp. 1-4.
38. B. Ebrahimi, H. Aghababa., and **A. Afzali-Kusha**, “Analytical Modeling of Read Stability Metric of SRAM Cell in Nanoscale era,” in *Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits*, Hong Kong, December 15-17, 2010, pp. 1-4.
39. A.-R. Ahmadi-Mehr, I. Madadi, and **A. Afzali-Kusha**, “A Subthreshold SRAM Cell Tolerant to Random Dopant Fluctuations,” in *Proceedings of IEEE International Conference of Electron Devices and Solid-State Circuits*, Hong Kong, December 15-17, 2010, pp. 1-4.
40. S.-N. Mozaffari and **A. Afzali-Kusha**, “Statistical model for subthreshold current considering process variations,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, Aug. 3 – 4, 2010, pp. 356 - 360.
41. S. Kiamehr, A.-R. Ahmadi-Mehr, S.-N. Mozaffari, and **A. Afzali-Kusha**, “A new block-based SSTA method considering within-die variation,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, Aug. 3 – 4, 2010, pp. 260 – 263.
42. F. Firouzi, S. Kiamehr, P. Monshizadeh, M. Saremi, **A. Afzali-Kusha**, and S.M. Fakhraie, “A model for transient fault propagation considering glitch amplitude and rise-fall time mismatch,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, Aug. 3 – 4, 2010, pp. 89 – 92.
43. M. Saremi, B. Ebrahimi, and **A. Afzali-Kusha**, “Process variation study of Ground Plane SOI MOSFET,” in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, Aug. 3 – 4, 2010, pp. 66 – 69.
44. M. Nickray and **A. Afzali-Kusha**, “ATC - An Asymmetric Topology Control Algorithm for Heterogeneous Wireless Sensor Networks” in *Proceedings of International Conference on Wireless Information Networks and Systems*, Seville, Spain, July 18 – 21, 2010, pp. 75 – 81.
45. H. Aghababa, **A. Afzali-Kusha**, and B. Forouzandeh, “Statistical Delay Modeling of Read Operation of SRAMs due to Channel Length Variation,” in *Proceedings of IEEE International Symposium on Circuits and Systems*, Paris, France, May 30 – June 2, 2010, pp. 2502 – 2505.
46. N. Ghobadi, **A. Afzali-Kusha**, and Ebrahim Asl-Soleimani, “Modeling of Hot Carrier Induced Substrate Current and Degradation in Triple Gate Bulk FinFETs,” in *Proceedings of 18th Iranian Conference on Electrical Engineering*, Isfahan, Iran, May 11-13, 2010, pp. 350-355.
47. N. Ghobadi, **A. Afzali-Kusha**, and Ebrahim Asl-Soleimani, “Modeling of Floating- Body Effect on Negative Bias Temperature Instability Degradation of Double-gate MOSFETs,” in *Proceedings of 18th Iranian Conference on Electrical Engineering*, Isfahan, Iran, May 11-13, 2010, pp. 356-361.

48. N. Ghobadi, R. Majidi, M. Mehran, and **A. Afzali-Kusha**, "Low Power 4-Bit Full Adder Cells in Subthreshold Regime," in *Proceedings of 18th Iranian Conference on Electrical Engineering*, Isfahan, Iran, May 11-13, 2010, pp. 362-367.
49. E. Rokhsat-Yazdi and **A. Afzali-Kusha**, "A High-Efficiency, Ripple-Control Buck Converter with Mode-Hop Enhancement," in *Proceedings of 2009 Second International Conference on Computer and Electrical Engineering*, Dubai, U.A.E., Dec. 28-30, 2009, pp. 443-447.
50. H. Aghababa, B. Forouzandeh, H. Dehghan, and **A. Afzali-Kusha**, "A robust method to estimate power and delay for digital integrated circuits," in *Proceedings of NORCHIP*, Trondheim, Norway, Nov. 16-17, 2009, pp. 1 – 5.
51. M. Nickray, M. Dehyadgari, and **A. Afzali-Kusha**, "Adaptive routing using context-aware agents for networks on chips," in *Proceedings of International Design and Test Workshop*, Nov. 15-17, 2009, Riyadh, Saudi Arabia, pp. 1 – 6.
52. H. Aghababa, **A. Afzali-Kusha**, and B. Forouzandeh, "Static power optimization of a Full-Adder under Front-End of Line systematic variations," in *Proceedings of International Design and Test Workshop*, Nov. 15-17, 2009, Riyadh, Saudi Arabia, pp. 1 – 6.
53. M. Saneei, M.R. Kakoei, and **A. Afzali-Kusha**, "COMRA: An efficient low-energy core mapping and routing path allocation algorithm for heterogeneous NoCs," in *Proceedings of International Design and Test Workshop*, Nov. 15-17, 2009, Riyadh, Saudi Arabia, pp. 1 – 6.
54. M. Nickray and **A. Afzali-Kusha**, "RATC: A robust topology control algorithm for heterogeneous wireless sensor networks," in *Proceedings of International Design and Test Workshop*, Nov. 15-17, 2009, Riyadh, Saudi Arabia, pp. 1 – 5.
55. H.R. Ahmadi and **A. Afzali-Kusha**, "Low-Power Low-Energy Prime-Field ECC Processor Based on Montgomery Modular Inverse Algorithm," in *Proceedings of Euromicro Conference on Digital System Design, Architectures, Methods and Tools*, Patras, Greece, Aug. 27-29, 2009, pp. 817 – 822.
56. B. Ebrahimi and **A. Afzali-Kusha**, "Realistic CNFET based SRAM cell design for better write stability," in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, July 15-16, 2009, pp. 14 – 18.
57. A.-R. Ahmadimehr, B. Ebrahimi, and **A. Afzali-Kusha**, "A high speed subthreshold SRAM cell design," in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, July 15-16, 2009, pp. 9 – 13.
58. N. Ghobadi, **A. Afzali-Kusha**, E. ; Asl-Soleimani, "Analytical modeling of Hot Carrier Injection induced degradation in triple gate bulk FinFETs," in *Proceedings of Asia Symposium on Quality Electronic Design*, Kuala Lumpur, Malaysia, July 15-16, 2009, pp. 28 – 34.
59. M. Gholipour, M. Nourani, D. Edwards, and **A. Afzali-Kusha**, "LLA: A low-latency asynchronous control with applications," in *Proceedings of International Symposium on Signals, Circuits and Systems*, Iasi, Romania, July 9-10, 2009, pp. 1 – 4.
60. H. R. Ahmadi and **A. Afzali-Kusha**, "Very low-power flexible GF(p) elliptic-curve crypto-processor for non-time-critical applications," in *Proceedings of IEEE International Symposium on Circuits and Systems*, Taipei, Taiwan, May 24-27, 2009, pp. 904 – 907.
61. S. Soleimani-Amiri, **A. Afzali-Kusha**, B. Forouzandeh, "High-temperature CNFET characteristics," in *Proceedings of International Conference on Thermal, Mechanical, and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems*, Delft, Netherland, April 26-29, 2009, pp. 1 – 4.

62. M. Ebrahimi, M. Daneshtalab, M. H. Neishaburi, S. Mohammadi, **A. Afzali-Kusha**, J. Plosila, and H. Tenhunen, "An Efficient Dynamic Multicast Routing Protocol for Distributing Traffic in NOCs," in *Proceedings of Design, Automation and Test in Europe*, Nice, France, 20-24 April, 2009, pp. 1064 - 1069.
63. S. Mohammadi and **A. Afzali-Kusha**, "An Efficient Threshold Voltage Model for Ultra Thin Body Double Gate/SOI MOSFETs," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16 – 18, 2009.
64. S. Mohammadi and **A. Afzali-Kusha**, "A Surface Field Based Model for Ultra Thin Body Undoped Symmetric DG MOSFETs," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16 – 18, 2009.
65. N. Ghobadi, **A. Afzali-Kusha**, and E. Asl-Soleimani, "Modeling Effect of Negative Bias Temperature Instability on Potential Distribution and Degradation of Double-gate MOSFETs," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16 – 18, 2009.
66. N. Ghobadi, **A. Afzali-Kusha**, and E. Asl-Soleimani, "Analytical Modeling of Negative Bias Temperature Instability in Triple Gate MOSFETs," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16–18, 2009.
67. S. Zeinolabedinzadeh, B. Ebrahimi, and **A. Afzali-Kusha**, " V_{th} -Control Method in Double Gate Field Effect Transistor Domino Circuits," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16–18, 2009.
68. B. Ebrahimi and **A. Afzali-Kusha**, "NBTI Tolerant 4T Double-Gate SRAM Design," in *Proceedings of Ultimate Integration on Silicon Conference*, Aachen, Germany, March 16 – 18, 2009.
69. B. Bozorgzadeh and **A. Afzali-Kusha**, "Novel MOS Decoupling Capacitor Optimization Technique for Nanotechnologies," in *Proceedings of International Conference on VLSI Design*, Jan. 5 – 9, 2009, New Delhi, India, pp. 175-180.
70. A.-M. Rahmani, I. Kamali, P. Lotfi-Kamran, **A. Afzali-Kusha**, S. Safari, "Negative Exponential Distribution Traffic Pattern for Power/Performance Analysis of Network on Chips," in *Proceedings of International Conference on VLSI Design*, Jan. 5 – 9, 2009, New Delhi, India, pp. 157-162.
71. A.-M. Rahmani, M. Daneshtalab, **A. Afzali-Kusha**, S. Safari, M. Pedram, "Forecasting-Based Dynamic Virtual Channels Allocation for Power Optimization of Network-on-Chips," in *Proceedings of International Conference on VLSI Design*, Jan. 5 – 9, 2009, New Delhi, India, pp. 151-156.
72. H.-R. Ahmadi and **A. Afzali-Kusha**, "Low-Power Flexible GF(p) Elliptic-Curve Cryptography Processor" in *Proceedings of 3rd International Design and Test Workshop*, Monastir, Tunisia, Dec. 20-22, 2008, pp. 182 – 186.
73. A.-M. Rahmani, M. Daneshtalab, **A. Afzali-Kusha**, and S. Safari "Power Efficient Switches with Dynamic Virtual Channel Allocation for Network-on-Chips," in *Proceedings of the 5th International Conference on Innovations in Information Technology*, Dubai, UAE, December 16-18, 2008.
74. A.-A. Salehpour, B. Mirmobin, **A. Afzali-Kusha**, and S. Mohammadi, "An Energy Efficient Routing Protocol for Cluster-Based Wireless Sensor Networks Using Ant Colony Optimization," in *Proceedings of the 5th International Conference on Innovations in Information Technology*, Dubai, UAE, December 16-18, 2008.
75. A.-A. Salehpour, **A. Afzali-Kusha**, and S. Mohammadi, "Efficient Clustering of Wireless Sensor Networks Based on Memetic Algorithm," in *Proceedings of the*

- 5th International Conference on Innovations in Information Technology, Dubai, UAE, December 16-18, 2008.
76. S. Soleimani, **A. Afzali-Kusha**, and B. Forouzandeh, "Temperature Dependence of Propagation Delay Characteristic in FinFET Circuits," in *Proceedings of the 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14-16, 2008, pp. 247-250.
 77. B. Bozorgzadeh, E. Zhian-Tabasi, and **A. Afzali-Kusha**, "Low-Power High-Performance Logic Style for Low-Voltage CMOS Technologies," in *Proceedings of the 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14-16, 2008, pp. 251-254.
 78. B. Bozorgzadeh and **A. Afzali-Kusha**, "Decoupling Capacitor Optimization for Nanotechnology Designs," in *Proceedings of the 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14-16, 2008, pp. 64-67.
 79. H. Hosseinzadegan, H. Aghababa, M. Zangeneh, **A. Afzali-Kusha**, and B. Forouzandeh, "A compact current-voltage model for carbon nanotube field effect transistors," in *Proceedings of International Semiconductor Conference*, Oct. 13 – 15, 2008, Sinaia, Romania, pp. 359 – 362.
 80. M. Gholipour, **A. Afzali-Kusha**, and M. Nourani, "A Novel Low Latency Asynchronous Pipeline Control Circuit," in *Proceedings of International Conference on Applied Electronics*, Sept. 10 – 11, 2008, Pilsen, Czech Republic, pp. 53-55.
 81. M.-R. Binesh-Marvasti, M. Daneshtalab, **A. Afzali-Kusha**, and S. Mohammadi, "PAMPR: Power-Aware and Minimum Path Routing Algorithm for NoCs," in *Proceedings of International Conference on Electronics, Circuits, and Systems*, Aug. 31 – Sept. 3, 2008, Malta, pp. 418 – 421.
 82. M. Hosseini, A. Jahanshahi, **A. Afzali-Kusha**, and B. Forouzandeh, "Modeling of Internal and External Fringe Capacitance Poly and Metal Gates in Nanoscale SOI CMOS Devices and Their Variations with Dielectric Constant," in *Proceedings of 16th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 14-16, 2008, pp. 6-12. (In Persian)
 83. M. Rostami, B. Ebrahimi, and **A. Afzali-Kusha**, "Design Centering Scheme for Robust SRAM Cell Design," in *Proceedings of International Conference on Computer and Communication Engineering*, May 13-15, 2008, Kuala Lumpur, Malaysia, pp. 871 – 877.
 84. B. Afzal, M. Rostami, M. Samadi, and **A. Afzali-Kusha**, "An Analytical Model for Threshold Voltage of FinFETs," in *Proceedings of International Conference on Computer and Communication Engineering*, May 13-15, 2008, Kuala Lumpur, Malaysia, pp. 760 – 763.
 85. H. Aghababa, M.H.A. Yazdinejad, **Afzali-Kusha**, and B. Forouzandeh, "Simplified Quantum-dot Cellular Automata Implementation of Counters," in *Proceedings of 7th International Caribbean Conference on Devices, Circuits and Systems*, Cancun, Mexico, April 28-30, 2008.
 86. H. Aghababa, N. Masoumi, **A. Afzali-Kusha**, and B. Forouzandeh, "Time-Domain Analysis of Carbon Nanotubes," in *Proceedings of 7th International Caribbean Conference on Devices, Circuits and Systems*, Cancun, Mexico, April 28-30, 2008.
 87. H. Aghababa, M. Jourabchian, **A. Afzali-Kusha**, and B. Forouzandeh, "Asynchronous circuits design using quantum-dot cellular automata for molecular computing," in *Proceedings of 7th International Caribbean Conference on Devices, Circuits, and Systems*, Cancun, Mexico, April 28-30, 2008.

88. B. Ebrahimi, S. Zeinolabedinzadeh, and **A. Afzali-Kusha**, "Low Standby Power and Robust FinFET Based SRAM Design," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, April 7 – 9, 2008, Montpellier, France, pp. 185-190.
89. H. Aghababa, M. Jourabchian, B. Forouzandeh, and **A. Afzali-Kusha**, "Asynchronous Circuits Design Using Quantum-dot Cellular Automata for Molecular Computing," in *Proceedings of Mosharaka International Conference on Communications, Propagation, and Electronics*, March 6-8, 2008, Amman, Jordan.
90. P. Lotfi, A.-M. Rahmani, A.-A. Salehpour, **A. Afzali-Kusha**, and Z. Navabi "Stall Power Reduction in Pipelined Architecture Processors," in *Proceedings of the 21st International Conference on VLSI*, Hyderabad, India, January 4-8, 2008, pp. 541-546.
91. M.A. Karami, **A. Afzali-Kusha**, R. Faraji-Dana, "Spontaneous Emission Modification Analysis of Hexagonally Shaped Nanowire Lasers," in *Proceedings of International Semiconductor Device Research Symposium*, December 12-14, 2007, College Park, Maryland.
92. H.-R. Zamani, M. Savadi-Oskoei, and **A. Afzali-Kusha**, "A Novel Method to Reduce Phase Noise in LC VCO Using a New Tail-Switching Technique," in *Proceedings of The International Workshop on Radio-Frequency Integration Technology*, December 9-11, 2007, Rasa Sentosa Resort, Singapore, pp. 94-97.
93. H.-R. Zamani and **A. Afzali-Kusha**, "A New Oscillator with Effective Phase-Noise/Power Performance," in *Proceedings of The International Workshop on Radio-Frequency Integration Technology*, December 09-11, 2007, Rasa Sentosa Resort, Singapore, pp. 98-101.
94. M. Samadi and **A. Afzali-Kusha**, "Power Management with Fuzzy Decision Support System," in *Proceedings of the 7th International Conference on ASIC*, October 26-29, 2007, Guilin, China, pp. 74-77.
95. M. Samadi, **A. Afzali-Kusha**, and C. Lucas, "Power Management by Brain Emotional Learning Algorithm," in *Proceedings of The 7th International Conference on ASIC*, October 26-29, 2007, Guilin, China, pp. 78-81.
96. M. A. Karami, M. Ahmadi-Boroujeni, **A. Afzali-Kusha**, and R. Faraji-Dana, "Semi-Analytic Model for Dispersion Relation of Nanowire Lasers," in *Proceedings of The 2nd International Conference on Nano-Networks*, September 24-26, 2007, Catania, Italy.
97. A. Jahanshahi, M. Hosseini, B. Esfandiarpour, and **A. Afzali-Kusha**, "Fringe Capacitance of Poly and Metal Gates in Nanoscale SOI CMOS Devices," in *Proceedings of Iran Physics Conference*, Aug. 26 – 29, 2007, Yasooj, Iran, pp. 899-902. (In Persian)
98. H. Hosseinzadegan, M. Moradinasab, B. Ebrahimi, **A. Afzali-Kusha**, and E. Arzi, "Deriving a Compact Model for Current-Voltage in Carbon Nanotube Field Effect Transistors in their Subthreshold Regime," in *Proceedings of Iran Physics Conference*, Aug. 26 – 29, 2007, Yasooj, Iran, pp. 907-910. (In Persian)
99. M.-R. Binesh-Marvasti, M. Saneei, and **A. Afzali-Kusha**, "Time-Efficient Power-Constrained Core Mapping Algorithm in NoC Based on Genetic Algorithm," in *Proceedings of the IEEE East-West Design & Test International Symposium*, September 7-10, 2007, Yerevan, Armenia, pp. 205-210.
100. M.-R. Binesh-Marvasti, S. Safari, **A. Afzali-Kusha**, and S. Mohammadi, "A Novel Fault-Tolerant Reconfigurable NoC Architecture," in *Proceedings of the*

- IEEE East-West Design & Test International Symposium*, September 7-10, 2007, Yerevan, Armenia, pp. 682-686.
101. B. Eghbalkhah, B. Afzal, and **A. Afzali-Kusha**, "Speed Improvement Algorithm for 16×16 Multipliers using Sizing Optimization," in *Proceedings of IEEE International Conference on Design & Technology of Integrated Systems*, Rabat, Morocco, September 2-5, 2007, pp. 102-105.
 102. B. Eghbalkhah, B. Bornoosh, Z. Amini-Sheshdeh, and **A. Afzali-Kusha**, "A New Preamble-less Timing Synchronization Method for OFDM Systems under Multi-Path Channels," in *Proceedings of IEEE International Conference on Design & Technology of Integrated Systems*, Rabat, Morocco, September 2-5, 2007, pp. 204-207.
 103. V. Moallemi and **A. Afzali-Kusha**, "Subthreshold Pass Transistor Logic for Ultra-Low Power Operation," in *Proceedings of 15th Iranian Conference on Electrical Engineering (Electronics)*, May 15-17, 2007, Tehran, Iran, pp. 138-143.
 104. Z. Jeddi, E. Amini, **A. Afzali-Kusha**, "Power-Driven Partitioning," in *Proceedings of 15th Iranian Conference on Electrical Engineering (Computer)*, May 15-17, 2007, Tehran, Iran, pp. 31-34.
 105. V. Moalemi and **A. Afzali-Kusha**, "Subthreshold 1-Bit Full Adder Cells in sub-100 nm Technologies," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, Porto Alegre, Brazil, May 9-11, 2007, pp. 514-515.
 106. V. Moalemi and **A. Afzali-Kusha**, "Subthreshold Pass Transistor Logic for Ultra-Low Power Operation," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, Porto Alegre, Brazil, May 9-11, 2007, pp. 490-491.
 107. M.A. Karami, **A. Afzali-Kusha**, R. Faraji-Dana, and M. Rostami, "Quantitative Comparison of Optical and Electrical H, X, and Y clock Distribution Networks," in *Proceedings of IEEE Computer Society Annual Symposium on VLSI*, Porto Alegre, Brazil, May 9-11, 2007, pp. 488 - 489.
 108. M. Savadi-Oskoei, **A. Afzali-Kusha**, S.M. Atarodi, "A High-Speed and Low-Power Voltage Controlled Oscillator in 0.18- μ m CMOS Process," in *Proceedings of IEEE International Symposium on Proceedings of Circuits and Systems*, May 27-30, 2007, Orlando, U.S.A., pp. 933-936.
 109. M. Daneshtalab, A. Pedram, M. H. Neishaburi, M. Riazati, **A. Afzali-Kusha**, and S. Mohammadi, "Distributing Congestions in NoCs through a Dynamic Routing Algorithm based on Input and Output Selections," in *Proceedings of International Conference on VLSI Design*, Bangalore, India, Jan. 6-10, 2007, pp. 546-560.
 110. M. Riazati, S. Mohammadi, **A. Afzali-Kusha**, and Z. Navabi, "Improved Assertion Lifetime via Assertion-Based Testing Methodology," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 48-51.
 111. H. Parandeh-Afshar, **A. Afzali-Kusha**, and A. Khakifirouz, "A Very Fast and Low Power Pseudo-Incrementer for Address Bus Encoder/Decoder," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 91-94.
 112. M. Dastjerdi-Mottaghi, A. Naghilou, **A. Afzali-Kusha**, Z. Navabi, and M. Daneshtalab, "Hot Block Ring Counter: A Low Power Synchronous Ring Counter," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 58-62.
 113. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, "A Mesochronous Technique for Communication in Network on Chips," in *Proceedings of the 18th International*

- Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 32-35.
114. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, "Low-latency Multi-Level Mesh Topology for NoCs," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 36-39.
 115. E. Rahmani, Z. Pajouhi, N. Kazemian-Amiri, and **A. Afzali-Kusha**, "Modified Leakage-Biased Domino Circuit with Low-Power and Low-Delay Characteristics," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 123-126.
 116. A.-S. Seyedi and **A. Afzali-Kusha**, "Double-edge Triggered Level Converter Flip-Flop with Feedback," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 44-47.
 117. M. A. Karami and **A. Afzali-Kusha**, "Adaptive Neural Network Model for SOI-MOSFET I-V Characteristics Including Self-Heating Effects," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 5-8.
 118. M. A. Karami and **A. Afzali-Kusha**, "Exponentially Tapering Ground Wires for Elmore Delay Reduction in On-Chip Interconnects," in *Proceedings of the 18th International Conference on Microelectronics*, Dhahran, Saudi Arabia, Dec. 17-19, 2006, pp. 99-102.
 119. A. Mehran, A. Khademzadeh, **A. Afzali-Kusha**, and B. Shirpour, "A Heuristic Energy Aware Application Mapping Algorithm for Network on Chip," in *Proceedings of IP Based SoC Design Conference & Exhibition*, Grenoble, France, Dec. 6-7, 2006, pp. 289-294.
 120. F. Aezinia, **A. Afzali-Kusha**, and C. Lucas, "Optimizing High Speed Flip-Flop Using Genetic Algorithm," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, Dec. 4-7, 2006, pp. 1789-1792.
 121. F. Aezinia, S. Najafzadeh, and **A. Afzali-Kusha**, "Novel High Speed and Low Power Single and Double Edge-Triggered Flip-Flops," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, Dec. 4-7, 2006, pp. 1413-1416.
 122. N. Honarmand and **A. Afzali-Kusha**, "Low Power Combinational Multiplier Using Data-driven Signal Gating," in *Proceedings of the IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, Dec. 4-7, 2006, pp. 1456-1459.
 123. M. Nazm-Bojnordi, N. Moezzi-Madani, M. Semsarzade, and **A. Afzali-Kusha**, "An Efficient Clocking Scheme for On-Chip Communications," in *Proceedings of The IEEE Asia Pacific Conference on Circuits and Systems*, Singapore, Dec. 4-7, 2006, pp. 119-122.
 124. P. Saeedi, A. Farmahini-Farahani, M. Hamzeh, and **A. Afzali-Kusha**, "Network-on-Chip Thermal-Balanced Mapping," in *Proceedings of International Design and Test (IDT) Workshop*, Dubai, U.A.E., November 19-21, 2006.
 125. M. Daneshtalab, S. Mohammadi, **A. Afzali-Kusha**, and O. Fatemi, "Minimizing Hot Spots in NoCs through a Dynamic Routing Algorithm based on Input and Output Selections," in *Proceedings of the International Symposium on System-on-Chip*, Tampere, Finland, Nov. 14-16, 2006, pp. 49-52.
 126. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, "Serial Bus Encoding for Low Power Application," in *Proceedings of The International Symposium on System-on-Chip*, Tampere, Finland, Nov. 14-16, 2006, pp. 99-102.
 127. M. Najibi, M. Salehi, **A. Afzali-Kusha**, M. Pedram, S.M. Fakhraie, and H. Pedram "Dynamic Voltage and Frequency Management Based on Variable Update

- Intervals for Frequency Setting,” in *Proceedings of the IEEE/ACM International Conference on Computer Aided Design*, San Jose, CA, Nov. 10-14, 2006, pp. 755-760.
128. M. Daneshtalab, A. Pedram, **A. Afzali-Kusha**, and S. Mohammadi, “A New Fair Dynamic Routing Algorithm for Avoiding Hot Spots in NoCs,” in *Proceedings of International Symposium on Communications and Information Technologies*, Bangkok, Thailand, October 18-20, 2006.
 129. M. Daneshtalab, A. Sobhani, **A. Afzali-Kusha**, O. Fatemi, and Z. Navabi, “NoC Hot Spot Minimization Using AntNet Dynamic Routing Algorithm,” in *Proceedings of the IEEE 17th International Conference on Application-specific Systems, Architectures and Processors*, Steamboat Springs, Colorado, September 11-13, 2006, pp. 33-38.
 130. A. Sobhani, M. Daneshtalab, M. H. Neishaburi, M. D. Mottaghi, **A. Afzali-Kusha**, O. Fatemi, and Z. Navabi, “Dynamic Routing Algorithm for Avoiding Hot Spots in On-chip Networks,” in *Proceedings of the IEEE International Conference on Design & Test Integrated Systems in Nanoscale Technology*, Tunis, Tunisia, Sept. 5-7, 2006, pp. 179-183.
 131. M. Daneshtalab, A. Sobhani, M. D. Mottaghi, **A. Afzali-Kusha**, Z. Navabi, and O. Fatemi, “Ant Colony Based Routing Architecture for Minimizing Hot Spots in NOCs,” in *Proceedings of the 19th Annual Symposium on Integrated Circuits and Systems Design (SBBCI)*, Ouro Preto, Brazil, Aug. 28 - Sept. 01, 2006, pp. 56-61.
 132. M. D. Mottaghi, **A. Afzali-Kusha**, and Z. Navabi, “ByZFAD: A Low Switching Activity Architecture for Shift-and-Add Multipliers,” in *Proceedings of the 19th Annual Symposium on Integrated Circuits and Systems Design (SBBCI)*, Ouro Preto, Brazil, Aug. 28 - Sept. 01, 2006, pp. 179-183.
 133. F. Aezinia, S. Najafzadeh, and **A. Afzali-Kusha**, “Novel High Speed and Low Power Single and Double Edge-Triggered Flip-Flops,” in *Proceedings of 3rd International Conference on Circuits and Systems for Communications*, Bucharest, Romania, July 6-7, 2006, pp. 19-22.
 134. F. Aezinia, **A. Afzali-Kusha**, C. Lucas, and S. Najafzadeh, “Optimizing High Speed Flip-Flop Using Genetic Algorithm,” in *Proceedings of 3rd International Conference on Circuits and Systems for Communications*, Bucharest, Romania, July 6-7, 2006, pp. 11-14.
 135. A.R. Aminlou, M.M. Khafaji, V. Moalemi, and **A. Afzali-Kusha**, “A Low-Power Low-Voltage Full Adder Cell using Latched XOR-XNOR,” in *Proceedings of 3rd International Conference on Circuits and Systems for Communications*, Bucharest, Romania, July 6-7, 2006, pp. 15-18.
 136. A. S. Seyedi, S. H. Rasouli, A. Amirabadi, **A. Afzali-Kusha**, C. Lucas, and B. Forouzandeh, “Design of Domino Logic Circuits by an Optimization Method,” in *Proceedings of Mixed Design of Integrated Circuits and Systems*, Gdynia, Poland, June 22-24, 2006, pp. 260-263.
 137. A.R. Saberhari, **A. Afzali-Kusha**, and Sh. Baradaran-Shokouhi, “Design of a Low-Power Low-Voltage 1-bit Adder Cell Using GDI Technique,” in *Proceedings of 14th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 16-18, 2006. (In Persian)
 138. S.G. Razavipour, S.A. Motamedi, and **A. Afzali-Kusha**, “Low-Power High-Speed SRAM Cell for Low-Power Applications,” in *Proceedings of 14th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 16-18, 2006.
 139. M. Salehi, M. Najibi, H. Pedram, **A. Afzai-Kusha**, and S.M. Fakhræi, “Implementation of DVFM Control System for Processor Power Reduction,” in

- Proceedings of 14th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 16-18, 2006. (In Persian)
140. A. Amirabadi, A. Chehelcheraghi, S. H. Rasouli, A. Seyedi, and **A. Afzali-Kusha**, "Low Power and High Performance Clock Delayed Domino Logic using Saturated Keeper in sub 100nm Technologies," in *Proceedings of 14th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 16-18, 2006.
 141. A. S. Seyedi, S. H. Rasouli, A. Amirabadi, and **A. Afzali-Kusha**, "Genetic Algorithm Method for Design of Domino Logic Circuits," in *Proceedings of 14th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 16-18, 2006.
 142. H. Parandeh-Afshar, **A. Afzali-Kusha**, and A. Khakifirooz, "A Very High Performance Address BUS Encoder," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 1731-1734.
 143. N. Honarmand, M.R. Javaheri, N. Sedaghati-Mokhtari and **A. Afzali-Kusha**, "Power Efficient Sequential Multiplication Using Pre-computation," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 2709-2712.
 144. B. Kheradmand-Boroujeni, F. Aezinia, and **A. Afzali-Kusha**, "High Performance Circuit Techniques for Dynamic OR Gates," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 3662-3666.
 145. S. Mehrmanesh, B. Eghbalkhah, S. Saeedi, **A. Afzali-Kusha**, and M. Atarodi "A Compact Low Power Mixed-Signal Equalizer for Gigabit Ethernet Applications," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 5167-5170.
 146. G. Razavipour, A. Motamedi, and **A. Afzali-Kusha**, "WL-VC SRAM: A Low Leakage Memory Circuit for Deep Sub-Micron Design," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 2237-2240.
 147. M. Riazati, A. Sobhani, M. Mottaghi-Dastjerdi, **A. Afzali-Kusha**, and A. Khakifirooz, "Low-Power Multiplier with Static Decision for Input Manipulation," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 2721-2724.
 148. M Saneei, **A Afzali-Kusha**, and Z Navabi, "Low-power and Low-latency Cluster Topology for Local Traffic NoCs," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 1727-1730.
 149. A. S. Seyedi, S. H. Rasouli, A. Amirabadi, and **A. Afzali-Kusha**, "Low Power Low Leakage Clock Gated Static Pulsed Flip-Flop," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 3658-3661.
 150. A. Amirabadi, A. Chehelcheraghi, S. H. Rasouli, A. Seyedi, and **A. Afzali-Kusha**, "Low Power and High Performance Clock Delayed Domino Logic using Saturated Keeper," in *Proceedings of 2006 IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 21-24, 2006, pp. 3173-3176.
 151. M. Dehyadgari, M. Nickray, **A. Afzali-Kusha**, and Z. Navabi, "A New Protocol Stack Model for Network on Chip," in the *Proceedings of IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*, March 2-3 2006, Karlsruhe, Germany, pp. 440 - 441.

152. A. S. Seyedi, S. H. Rasouli, A. Amirabadi, and **A. Afzali-Kusha**, "Clock Gated Static Pulsed Flip-Flop (CGSPFF) in Sub 100 nm Technology," in the *Proceedings of IEEE Computer Society Annual Symposium on Emerging VLSI Technologies and Architectures*, March 2-3, 2006, Karlsruhe, Germany, pp. 373 - 377.
153. S. H. Rasouli, A. Amirabadi, A. S. Seyedi, and **A. Afzali-Kusha**, "Double Edge Triggered Feedback flip-flop in Sub 100nm Technology," in the *Proceedings of Asia and South Pacific Conference on Design Automation*, Jan. 24-27 2006, Yokohama, Japan, pp. 297 - 302.
154. P. Hashemi, J. Derakhshandeh, S. Mohajerzadeh, M.D. Robertson, J.C. Bennett, A. Shayan-Arani, and **A. Afzali-Kusha**, "Characterization of Low Temperature Stress-Induced Crystallization of a-Si on Flexible Glass Substrate by Transmission Electron Microscopy and Raman Spectroscopy," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 326-329.
155. M. Nazm-Bojnordi, M. Semsarzadeh, A. Banaiyan, and **Ali Afzali-Kusha**, "A Simple, Low-Cost and Low-Power Switch Architecture for NoCs," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 194-197.
156. M. Dehyadgari, M. Nickray, **A. Afzali-Kusha**, and Z. Navabi, "Evaluation of Pseudo Adaptive XY Routing Using an Object Oriented Model for NOC," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 204-208.
157. M. Nickray, M. Dehyadgari, A. Sobhani, and **A. Afzali-Kusha**, "Multiplier for Correlative Input Patterns," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 72-74.
158. V. Majidzadeh, S. M. Alavi, and **A. Afzali-Kusha**, "Design of Merged Differential Cascode Voltage Switch with Pass-Gate (MDCVSPG) Logic for High-Performance Digital Systems," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 63-66.
159. B. Kheradmand-Boroujeni, A. Seyyedi, and **A. Afzali-Kusha**, "High Speed Low Gate Leakage Large Capacitive-Load Driver Circuits for Low-Voltage CMOS," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 30-35.
160. B. Kheradmand-Boroujeni, K. Shojaee, and **A. Afzali-Kusha**, "Design and Simulated Annealing Optimization of a Static Comparator for Low-Power High-Speed CMOS VLSI," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 355-359.
161. B. Kheradmand-Boroujeni and **A. Afzali-Kusha**, "A New Static High Fan-In OR-NOR Gate Structure Suitable for Low Power CMOS VLSI," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 102-105.
162. A. Amirabadi, Y. Mortazavi, and **A. Afzali-Kusha**, "An Efficient Forward Biasing Body Bias Generator for Clock Delayed Domino Logic," in *Proceedings of the 17th International Conference on Microelectronics*, Islamabad, Pakistan, December 13-15, 2005, pp. 13-18.
163. M. Dehyadgari, M. Nickray, and **A. Afzali-Kusha**, "Power and Delay Optimization for Network on Chip," in *Proceedings of European Conference on*

- Circuit Theory and Design (ECCTD'05)*, Cork, Ireland, Aug. 28-Sept. 2, 2005, pp. III-277-III-281.
164. M. Dehyadgari, M. Nickray, and **A. Afzali-Kusha**, "Low Power Communication for Network on Chip," in *Proceedings of International Symposium on Telecommunications (IST'05)*, Shiraz, Iran, Sept. 10-12, 2005, pp. 521-525.
 165. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, "Sign Bit Reduction Encoding For Low Power Applications," in *Proceedings of 42nd Design Automation Conference*, Anaheim, U.S.A., June 13-17, 2005, pp. 213-217.
 166. A. Abbasian, M. Taherzadeh-Sani, B. Amelifard, and **A. Afzali-Kusha**, "Modeling of MOS Transistors Based on Genetic Algorithm and Simulated Annealing," in *Proceedings of 2005 IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 6218-6221.
 167. B. Afzal, **A. Afzali-Kusha**, and M. El Nokali, "Efficient Power Model for Crossbar Interconnects," in *2005 Proceedings of IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 5858-5861.
 168. B. Amelifard, **A. Afzali-Kusha**, and A. Khademzadeh, "Enhancing the Efficiency of Cluster Voltage Scaling Technique for Low-power Applications," in *Proceedings of 2005 IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 1666-1669.
 169. A. Amirabadi, Y. Mortazavi, N. Moezzi-Madani, **A. Afzali-Kusha**, and M. Nourani, "Domino Logic with an Efficient Variable Threshold Voltage Keeper," in *Proceedings of 2005 IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 1674-1677.
 170. M. Gholipour, K. Shojaee, **A. Afzali-Kusha**, A. Khademzadeh, and M. Nourani, "An Efficient Model for Performance Analysis of Asynchronous Pipeline Design," in *Proceedings of 2005 IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 5236-5239.
 171. S. Hatami, M. Alisafaei, E. Atoofian, Z. Navabi, and **A. Afzali-Kusha**, "A Low-Power Scan-Path Architecture," in *2005 IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May 23-26, 2005, pp. 5278-5281.
 172. A. Amirabadi, Y. Mortazavi, and **A. Afzali-Kusha**, "Clock Delayed Domino Logic with an Efficient Variable Voltage Keeper Threshold," in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 416-420.
 173. R. Safa-Isini, G. Razavipour, and **A. Afzali-Kusha**, "A Self-Controllable Voltage Level Circuit with Body Biasing for Low Power Applications," in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 167-171. (In Persian)
 174. S. Toofan, **A. Afzali-Kusha**, A. Ale-Ahmad, and A. Rahmati "New Current Mode Amplifier for Low-Power Low-Voltage SRAMs in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 109-112. (In Persian)
 175. A.A. Shirazai-Beheshti, E. Rouhani, K. Abdi, and **A. Afzali-Kusha**, "Improved Alpha-Power Model For MOSFETs," in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 79-84. (In Persian)
 176. M. Nickray, M. Dehyadgari, A. Sobhani, and **A. Afzali-Kusha**, "LPPM: Low Power Partitioned Multiplier," in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005.
 177. V. Majidzadeh, S. M. Alavi, and **A. Afzali-Kusha**, "Design of Merged Differential Cascade Voltage Switch with Pass-Gate (MDCVSPG) Logic for

- High-Performance Digital Systems,” in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005.
178. B. Afzal and **A. Afzali-Kusha**, “Speed Improvement of 16×16 Multipliers using Sizing Optimization by Genetic Algorithm,” in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 130-134.
 179. B. Afzal and **A. Afzali-Kusha**, “Optimized Design of Wallace Tree in Direct Form Block by Genetic Algorithm,” in *Proceedings of 13th Iranian Conference on Electrical Engineering*, Zanjan, Iran, May 10-12, 2005, pp. 321-325. (In Persian)
 180. S. Sharifi, J. Jaffari, A. Hosseinabadi, **A. Afzali-Kusha**, and Z. Navabi, “Simultaneous Reduction of Dynamic and Static Power in Scan Structures,” in *Proceedings of the Design, Automation and Test in Europe*, March 7-11, Munich, Germany, 2005, pp. 846 - 851. (In Persian)
 181. M. Alisafae, S. Hatami, E. Atoofian, Z. Navabi and **A. Afzali-Kusha**, “Architecture of a Data Compression-based Low-power Scan-path,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, 2004, pp. 768-771.
 182. M. Saneei, **A. Afzali-Kusha**, and Z. Navabi, “A Low Power Technique Based on Sign Bit Reduction,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, 2004, pp. 497-500.
 183. A. Amirabadi, Y. Mortazavi, and **A. Afzali-Kusha**, “Optimizing Low-Power High-Speed Full Adders With Simulated Annealing,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 429-432, 2004.
 184. J. Jaffari and **A. Afzali-Kusha**, “New Dual-Threshold Voltage Assignment Technique for Low-Power Digital Circuits,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 413-416, 2004.
 185. M. Gholipour, K. Shojae, A. Khademzadeh, **A. Afzali-Kusha**, and M. Nourani, “Performance and Power Analysis of Asynchronous Pipeline Design Methods,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 409-412, 2004.
 186. P. Hashemi, A. Behnam, E. Fathi, and **A. Afzali-Kusha**, “Two-Dimensional Analytical Modeling and Simulation of the Potential and Threshold Voltage of a New Fully Depleted Dual Metal Gate SOI MESFET,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 372-375, 2004.
 187. M. Taherzadeh-Sani, A. Abbasian, B. Amelifard, and **A. Afzali-Kusha**, “MOS Compact I-V Modeling with Variable Accuracy Based on Genetic Algorithm and Simulated Annealing,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 364-367, 2004.
 188. B. Afzal and **A. Afzali-Kusha** “Power Estimation of Crossbar Interconnects Using Fully Analytical Approach,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 219-222, 2004.
 189. J. Jaffari and **A. Afzali-Kusha**, “A Novel Technique for Reducing Leakage Current of VLSI Combinational Circuits,” in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 207-210, 2004.

190. N. Moezzi-Madani, B. Tavassoli, A. Behnam, and **A. Afzali-Kusha**, "Study of Super Cut-Off CMOS Technique in Presence of the Gate Leakage Current," in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 24-27, 2004.
191. F. Farbiz, A. Behnam, M. Emadi, B. Esfandiarpour, and **A. Afzali-Kusha**, "Voltage and Sizing Optimization for Low Power Buffered Digital Designs," in *Proceedings of the 16th International Conference on Microelectronics*, Tunis, Tunisia, December 6-8, pp. 20-23, 2004.
192. M. H. Tehranipour, M. Nourani, K. Arabi and **A. Afzali-Kusha**, "Mixed RL-Huffman Encoding for Power Reduction and Data Compression in Scan Test," in *Proceedings of 2004 IEEE International Symposium on Circuits and Systems*, Vancouver, Canada, May 23-26, pp. II681-II684, 2004.
193. A. Abbasian, S. Hatami, **A. Afzali-Kusha**, M. Nourani, and C. Lucas "Event-Driven Dynamic Power management Based on Wavelet Forecasting Theory," in *Proceedings of 2004 IEEE International Symposium on Circuits and Systems*, Vancouver, Canada, May 23-26, pp. V325-V328, 2004.
194. A. Abbasian, S. Hatami, **A. Afzali-Kusha**, C. Lucas, and M.R. Zamani, "Wavelet Based Dynamic Power Management for Nonstationary Service Requests," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 226-231.
195. B. Afzal, E. Fathi, A.L. Baghestani, **A. Afzali-Kusha**, and M. Nourani, "Power Estimation of Crossbar Interconnect using Fully Analytical Approach," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 192-197.
196. A. Zahabi, Y. Koolivand, **A. Afzali-Kusha**, and M. Nourani, "Area and Power Optimization Method for High-Speed Dual VT Domino Logic with Noise Constraint," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 103-108.
197. J. Jafari, A. Amirabadi, and **A. Afzali-Kusha**, "A Novel Technique for Reducing Subthreshold Current of VLSI Combinational Circuits," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 163-167.
198. A. Amirabadi, R.A. Tousi, J. Jafari, and **A. Afzali-Kusha**, "Leakage Current Reduction by New Technique in Standby Mode," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 46-51.
199. S. H. Rasouli, **A. Afzali-Kusha**, A. Khademzadeh, and M. Nourani, "Double Edge Triggered Modified Hybrid Latch Flip-flop (DMHLFF)," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 139-144.
200. S.H. Rasouli, **A. Afzali-Kusha**, A. Khademzadeh, M.H. Tehranipour, M. Nourani "A New Test Pattern Generator by Altering the Structure of 2-D LFSR for Built-in Self Test Applications," in the *Proceedings of 12th Iranian Conference on Electrical Engineering*, Mashhad, Iran, May 11-13, 2004, vol. 1, pp. 259-264.
201. D. Shahrjerdi, B. Hekmatshoar, **A. Afzali-Kusha**, and A. Khakifirooz, "Optimization of the VT-Control Method for Low-Power Ultra-Thin Double-Gate SOI Logic Circuits," in *Proceedings of The 2004 Great Lakes Symposium on VLSI (GLSVLSI'04)*, pp. 236-239, April 26-28, 2004, Boston, Massachusetts, U.S.A.

202. A. Amirabadi, J. Jafari, **A. Afzali-Kusha**, M. Nourani, and A. Khakifirooz, "Leakage Current Reduction by New Technique in Standby Mode," in Proceedings of The 2004 Great Lakes Symposium on VLSI (GLSVLSI'04), pp. 158-161, April 26-28, 2004, Boston, Massachusetts, U.S.A.
203. R. Dehghani, S.M. Atarodi, B. Bornoosh, and **A. Afzali Kusha**, "A Reduced Complexity 3rd Order Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesis," in Proceedings of the 17th International Conference on VLSI Design, January 05-09, 2004, pp. 615-618, Mumbai, India.
204. A. Abbasian, A.M. Nasri-Nasr Abadi, and **A. Afzali-Kusha**, "Modular Energy Recycling Differential Logic (MERDL) for Low Power Applications," in Proceedings of 10th IEEE International Conference on Electronics, Circuits and Systems, Dec. 14-17, 2003, Sharjah, United Arab Emirates, 2003, pp. 312-315.
205. A. Abbasian and **A. Afzali-Kusha**, "Pipeline Event-driven No-race Charge Recycling Logic (PENCL) for Low Power Applications," in Proceedings of 10th IEEE International Conference on Electronics, Circuits and Systems, Dec. 14-17, 2003, pp. 220-223, Sharjah, United Arab Emirates, 2003.
206. S. H. Rasouli, **A. Afzali-Kusha**, A. Khademzadeh, and M. Nourani, "Low-Race Split-level Charge-Recycling Pass-Transistor Logic (LSCPL) for Low Power High Speed Applications," in Proceedings of the 15th International Conference on Microelectronics, Dec. 9-11, 2003, Cairo, Egypt, 2003, pp. 243-246.
207. H. R. Bahrami, A.M. Nasri-Nasrabadi, S.H.R. Jamali, and **A. Afzali-Kusha**, "Manipulation of Antenna Correlation for the Capacity Enhancement in MIMO Communication Systems," in Proceedings of 2003 Australian Telecommunications, Networks and Applications Conference (ATNAC), December 8-10, 2003, Melbourne, Australia.
208. A.M. Nasri-Nasrabadi, H.R. Bahrami, S.H.R. Jamali, and **A. Afzali-Kusha**, "Effect of Antenna Separation on Capacity and Performance of MIMO Systems," in Proceedings of 2003 Australian Telecommunications, Networks and Applications Conference (ATNAC), December 8-10, 2003, Melbourne, Australia.
209. B. Hekmatshoar, D. Shahrjerdi, S. Mohajerzadeh, A. Khakifirooz, M. Robertson, and **A. Afzali-Kusha**, "Stress-Assisted Copper-induced Lateral Growth of Polycrystalline Germanium," in Proceedings of 2003 MRS Fall Meeting, vol. 795, pp. 199-204, December 1-5, Boston, MA, 2003.
210. E. Atoofian, S. Hatami, Z. Navabi, M. Alisafae, and **A. Afzali-Kusha**, "A New Low-Power Scan-Path Architecture," IEEE 4th Workshop on RTL and High Level Testing, pp. 91-95, November 20-21, 2003, XI'AN, China.
211. M. Naderi, B. Javadi, H. Pedram, **A. Afzali-Kusha**, and M. K. Akbari, "An Asynchronous Viterbi-Decoder for Low-Power Applications", in Proceedings of International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS 2003), Torino, Italy, September 10-12, pp. 471-480, Italy, Sep. 2003.
212. M. H. Tehranipour, M. Nourani, S. M. Fakhraie, and **A. Afzali-Kusha**, "Systematic Test Program Generation for SoC Testing Using Embedded Processor," in Proceedings of 2003 IEEE International Symposium on Circuits and Systems, pp. V541-V544, Bangkok, Thailand, May 25-28, 2003.
213. M. Yavari, O. Shoaie, and **A. Afzali-Kusha**, "A Very Low-Voltage, Low-Power and High Resolution Sigma-Delta Modulator for Digital Audio in 0.25- μ m CMOS," in Proceedings of 2003 IEEE International Symposium on Circuits and Systems, pp. I1045-I1048, Bangkok, Thailand, May 25-28, 2003.

214. A. Abbasian, S.H. Rasouli, **A. Afzali-Kusha**, and M. Nourani, "No-race Pass Transistor Logic (NCRPL) for Low Power Applications," in Proceedings of 2003 IEEE International Symposium on Circuits and Systems, pp. V289-V292, Bangkok, Thailand, May 25-28, 2003.
215. B. Amelifard, M. Taherzadeh-Sani, H. Iman-Eini, and **A. Afzali-Kusha**, "Delay and Power Estimation of CMOS Inverters," in Proceedings of 11th Iranian Conference on Electrical Engineering, Shiraz, May 6-8, 2003, vol. 1, pp. 458-464.
216. H. Iman-Eini, M. Taherzadeh-Sani, B. Amelifard, and **A. Afzali-Kusha**, "Reducing CMOS Gates to Equivalent Inverters Based on Modified n -th Power Law MOSFET Model," in the Proceedings of 11th Iranian Conference on Electrical Engineering, Shiraz, Iran, May 6-8, 2003, vol. 1, pp. 452-457.
217. T. Maleki, B. Sadeghi, E. YousefNezhad, M. GhafouriFard, S. MohajerZadeh, **A. Afzali-Kusha**, and E. Asl-Soleimani, "Non-isotropic etching of PET using UV," in the Proceedings of 11th Iranian Conference on Electrical Engineering, Shiraz, Iran, May 6-8, 2003, vol. 1, pp. 159-166. (in Persian).
218. S.H. Rasouli, A. Abbasian, **A. Afzali-Kusha**, and A. Khademzadeh, "MRFCPL: A new charge recycling logic with no sensitivity to signal skew for low-power applications," in the Proceedings of 11th Iranian Conference on Electrical Engineering, Shiraz, Iran, May 6-8, 2003, vol. 1, pp. 26-33. (in Persian).
219. M. Nourani, **A. Afzali-Kusha**, J. Carletta, and C. Papachristou "Effect of Don't Cares on SoC's Testability and Power," in Proceedings of 8th Annual International Computer Society of Iran Computer Conference, Mashad, Iran, Feb. 25-27, pp. 60-67, 2003.
220. M. Taherzadeh-Sani, H. Iman-Eini, B. Amelifard, M. Farazian, **A. Afzali-Kusha**, and M. Nourani "A simple yet accurate analytical method for reducing CMOS gates to equivalent inverters," in Proceedings of the 2003 Southwest Symposium on Mixed-Signal Design, Las Vegas, U.S.A., 23-25 February, pp. 116-120, 2003.
221. M. Taherzadeh-Sani, B. Amelifard, H. Iman-Eini, F. Farbiz, **A. Afzali-Kusha**, and M. Nourani "Power and Delay Estimation of CMOS Inverters Using Fully Analytical Approach," in Proceedings of the 2003 Southwest Symposium on Mixed-Signal Design, Las Vegas, U.S.A., 23-25 February, pp. 112-115, 2003.
222. A. Abbasian, S.H. Rasouli, J. Derakhshandeh, **A. Afzali-Kusha**, and M. Nourani "Race-free CMOS PASS-gate Charge Recycling Logic (FCPCL) For Low Power Applications," in Proceedings of the 2003 Southwest Symposium on Mixed-Signal Design, Las Vegas, U.S.A., 23-25 February, 2003, pp. 87-89, 2003.
223. S. Hatami, M.Y. Azizi, H.R. Bahrami, D. Motavalizadeh and **A. Afzali-Kusha**, "Modeling of Drain Current Characteristics of SOI MOSFETs Using Neural Networks," in Proceedings of the 14th International Conference on Microelectronics, Beirut, Lebanon, December 11-13, pp. 114-117, 2002.
224. M. Maddah, S. Bolouki, **A. Afzali-Kusha**, and M. El-Nokali "A Compact Modeling of Drain Current in PD/FD SOI MOSFETs," in Proceedings of the 14th International Conference on Microelectronics, Beirut, Lebanon, December 11-13, pp. 75-78, 2002.
225. M. Nourani, S. Nazarian, and **A. Afzali-Kusha**, "A Parallel Algorithm for Power Estimation at Gate Level," in *Proceedings of the 45th IEEE International Midwest Symposium on Circuits and Systems*, Tulsa, Oklahoma, August 4-7, 2002.
226. M. Gholipour, **A. Afzali-Kusha**, M. Nourani, and A. Khademzadeh, "An Efficient Asynchronous Pipeline FIFO for Low-Power Applications," in *Proceedings of the 45th IEEE International Midwest Symposium on Circuits and Systems*, Tulsa, Oklahoma, August 4-7, 2002.

227. M. Maddah, **A. Afzali-Kusha**, H. Soltanian-Zadeh, "Efficient Medial Curve Extraction of Microvascular Structures in Confocal Microscopy Images," in *Proceedings of International Conference on Diagnostic Imaging and Analysis*, Shanghai, China, 18-20 August, 2002.
228. M. Maddah, **A. Afzali-Kushaa**, H. Soltanian-Zadeh, "Fast centerline extraction for quantification of vessels in Confocal Microscopy images," in *Proceedings of 2002 IEEE International Symposium on Biomedical Imaging*, Washington, D.C., 7-10 July, 2002.
229. H. Mahmoodi-Meimand and **A. Afzali-Kusha**, "Efficient Power Clock Generation For Adiabatic Logic," in *Proceedings of 2001 IEEE International Symposium on Circuits and Systems*, Sydney, Australia, May 6-9, 2001.
230. H. Mahmoodi-Meimand and **A. Afzali-Kusha**, "Low-Power, Low-Noise Adder Design with Pass-transistor Adiabatic Logic," in *Proceedings of International Conference of Microelectronics*, Tehran, Iran, Oct. 31- Nov. 2, 2000, pp. 61-64.
231. S. M.-J. Okhovat-Alavian, **A. Afzali-Kusha**, and M. Kamarei, "Intersubband Transitions in Different Structures of Conduction-Band Quantum Wells," in *Proceedings of International Conference of Microelectronics*, Tehran, Iran, Oct. 31- Nov. 2, 2000, pp. 181-186.
232. H. Mahmoodi-Meimand, **A. Afzali-Kusha**, and M. Nourani, "Efficiency of Adiabatic Logic for Low-Power, Low-Noise VLSI," in *Proceedings of Midwest Symposium on Circuits and Systems*, Lansing, Michigan, August 2000.
233. M.R. Famil-Khodaei, **A. Afzali-Kushaa**, and M.H. Miranbeigi, "Simulation of the water vapor effect in determining temperature tissue distribution under Nd:YAG laser light using the Monte-Carlo method and neural network," in *Proceedings of the 7th Iranian Conference on Electrical Engineering*, Tehran, Iran, May 1999, Biomedical Engineering Proceedings, pp. 49-57. (in Persian).
234. M.R. Famil-Khodaei, **A. Afzali-Kushaa**, and M.H. Miranbeigi, "Determining the suitable wavelength for the treatment of PWS using the Monte-Carlo simulation of the laser light propagation in the tissue," in *Proceedings of the 7th Iranain Conference on Electrical Engineering*, Tehran, Iran, May 1999, Biomedical Engineering Proceedings, pp. 33-40. (in Persian).
235. C.Y. Sung, **A. Afzali-Kushaa**, T.B. Norris, X. Zhang, and G.I. Haddad, "Time-resolved femtosecond intersubband relaxations and population inversion in stepped quantum wells," in *Proceedings of Hot Carriers in Semiconductors*, July 31-Aug. 4, 1995; Chicago, IL, USA, pp. 37-41.
236. X. Zhang, G.I. Haddad, J.P. Sun, C.Y. Sung, **A. Afzali-Kushaa**, and T.B. Norris, "Population inversion in step quantum wells at 10 mm wavelength," in *Proceedings of 53rd Annual Device Research Conference*, Charlottesville, Virginia, June 19-21, 1995, pp. 118-119.
237. **A. Afzali-Kushaa** and G.I. Haddad, "Lasers Based on Intersubband Transitions in Quantum Wells," (Keynote Address), *SPIE vol. 2397 -- Optoelectronic Integrated Circuits Materials Physics and Devices*, April 1995, pp. 476-494.
238. T.B. Norris, C.Y. Sung, **A. Afzali-Kushaa**, and G.I. Haddad, "Intersubband Relaxation and Population Inversion in Stepped Quantum Wells," in *Proceedings of Ultrafast and Optoelectronics and Quantum Optoelectronics Conference*, Dana Point, California, March 13-15, 1995.
239. X. Zhang, **A. Afzali-Kushaa**, W.L. Chen, G. Munns, and G.I. Haddad, "Absorption and Population Inversion in p-type InGaAs Strained Layers Based on Intervalence Subband Transitions at FIR Frequencies," in *Proceedings of 6th*

- International Conference on Infrared Physics*, May 29-June 3, 1994, Ticino, Switzerland, pp. 151-153.
240. **A. Afzali-Kushaa**, G.I. Haddad, and T.B. Norris, "Optically Pumped Intersubband Lasers," in *Proceedings of 1993 International Semiconductor Device Research Symposium*, December 1-3, 1993, Charlottesville, Virginia.
 241. X. Zhang, P. Liao, **A. Afzali-Kushaa**, and G.I. Haddad, "Interband Absorption in p-type InGaAs at FIR Frequencies," in *Proceedings of 1993 MRS Fall Meeting*, November 29-December 2, 1993, Boston, Massachusetts, pp. 69-73.
 242. **A. Afzali-Kushaa**, G.I. Haddad, and T.B. Norris, "On the Feasibility of Intersubband Transition Lasers," in *Proceedings of IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Device and Circuits*, August 2-4, 1993, Ithica, New York, pp. 167-176.
 243. **A. Afzali-Kushaa**, G.I. Haddad, and T.B. Norris, "THz Sources Based on Intersubband Transitions in Quantum Wells and Strained Layers," in *Proceedings of Fourth International Symposium on Space Terahertz Technology*, March 30-April 1, 1993, UCLA, Los Angeles, California, pp. 573-587.
 244. M. El-Nokali and **A. Afzali-Kushaa**, "A Subthreshold Model for the Analysis of MOS IC's," in *Proceedings of Ninth Biennial University/Government/Industry Microelectronics Symposium*, June 12-14, 1991, Melbourne, Florida, pp. 169-172.
 245. **A. Afzali-Kushaa** and M. El-Nokali, "A CAD Model for MOS Transistors Valid in All Regions of Operation," in *Proceedings of 34th Midwest Symposium on Circuits and Systems*, May 14-17, 1991, Monterey, California, pp. 364-367.
 246. **A. Afzali-Kushaa** and M. El-Nokali, "Issues Related to the Modeling of MOS Transistors in Subthreshold," in *Proceedings of 22nd Annual Pittsburgh Conference on Modeling and Simulation*, vol. 22, part 2: *Expert Systems, Artificial Intelligence, Electronic Databases, Hydrology, Manufacturing*, May 3-5, 1991, Pittsburgh, Pennsylvania, pp. 921-928.

