

Letter of Motivation (Statement of Purpose)

Dear Sir/Madam;

My name is **Mohsen Ansari** and I wish to request for a non-resident researcher in IPM.

Looking back at my academic life, I acquired the B.Sc. degree in computer engineering from Shahed University, Tehran, Iran, in 2014. I received the PhD and M.Sc. degrees in computer engineering from Sharif University of Technology, Tehran, Iran, in 2016 and 2021, respectively. I am currently the assistant professor of computer engineering in Sharif University of Technology, Tehran, Iran, from 2022 up to now.

I want to work on dependable cyber-physical systems at IPMZ. Modern CPSs due to continuing the scaling of feature size are thermally constrained. Technology scaling allows more transistors to be integrated onto a multicore chip. The chip-level power constraint, Thermal Design Power (TDP), is the highest sustainable power that a chip can dissipate to avoid performance throttling mechanisms. However, TDP as the power constraint of a system can be very pessimistic, therefore, having better power budget is a major requirement towards dealing with performance losses. A new power budget concept called Thermal Safe Power (TSP) provides safe and efficient power constraint. If the peak power consumption of each processing core violates its TSP, it automatically restarts or significantly reduces its performance to prevent a permanent damage. Therefore, dissipating power consumption of cores below TSP results in maximum (safe) temperature such that performance throttling mechanism is not triggered. TSP is computed in the offline phase for the worst-case scenarios, or unlike TDP in the online phase for a specific mapping of cores. When core heterogeneity or timing guarantees are involved, TSP can also guide task partitioning and mapping decisions. In order to meet the TDP/TSP constraints, some solutions like heat-sink and chip's cooling are proposed while due to their negative effects on the system reliability these solutions are not used in dependable CPSs. Therefore, peak power minimization is an efficient way to meet the TDP and TSP constraints and prevent the system from producing high temperature. Another limitation of CPSs is that most of them are battery-based, and hence, the energy consumption of them should be reduced. Energy is the integration of power consumption through time while the peak power consumption is the instantaneous power consumption. Therefore, existing energy minimization schemes are unsuitable for peak power reduction and vice versa. In summary, we want to prolong battery lifetime and meet the chip/core power constraints which are two major issues in modern embedded systems.

Thank you very much indeed for your consideration of my case in advance. I look forward to hearing from you.

Yours Faithfully;

Mohsen Ansari