CD-DFT: A Current-Difference Design-for-Testability to Detect Short Defects of STT-MRAM Under Process Variations

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***Abstract*—This work presents an efficient test technique for detecting resistive short defects in STT-MRAM arrays. The proposed technique is based on monitoring the current mismatch flowing into and out of the cell caused by a weak or strong short defect. This technique is used to propose a low area overhead Design-for-Testability (DFT) circuit to employ in STT-MRAM arrays to distinguish defect-free cells from faulty ones. The operation of the proposed test approach is resilient to the parameter uncertainties of the array circuit induced by process variations. The variations, however, may lower defect detection ranges. The efficacies of the proposed DFT technique under the nominal and the process variation cases are studied. Simulation results indicate that the proposed DFT circuit reduces the number of test escapes and improves the fault coverage by a factor of at least 10× (5×) under short defect to ground (short defect to V_{DD}) cases compared to the corresponding maximum ones detected by conventional test schemes. The technique works through a single read operation with a negligible area overhead, especially, in large size arrays.**

***Index Terms*—Design for testability, process variations, short defects, STT-MRAM.**

I. Introduction

CONVENTIONAL memory technologies, such as Static Random-Access Memory (SRAM), are facing major issues such as the looming end of Moore's law and reaching the classical limit of device miniaturization [1]. This type of issues has been the driving force behind new memory technologies. The Spin-Transfer-Torque Magnetic RAM (STT-MRAM) is an emerging non-volatile memory technology which has the best compatibility with planar MOSFET and FinFET processes [1], [2]. STT-MRAM has great advantages of scalability, high endurance, high speed, and low-power dissipation [3], [4]. These features have been the main reasons for this technology being adopted by different foundries [5]. Due to its superior features like better controllability of the active region by the gate and lower vulnerability to manufacturing process variations compared to the planar MOSFET, FinFET transistors are employed as the access transistor when fabricating the STT-MRAM cells [2].

The characteristic variability of STT-MRAM induced during the manufacturing process is attributed to typical defects that disturb read/write operation leading to weak or strong faults [6], [7]. Strong faults lead to functional errors and can be detected by standard test methods [8]. Weak faults, however, cause only parametric changes in the circuits with no logical error [8]. The manufacturing defects are classified into inter-cell and intra-cell defects in which all of inter-cell and most of intra-cell defects are modeled as resistive shorts [7]. Moreover, due to technology scaling, the sensitivity of a circuit under test to resistive-short defects (modeled as a resistive connection between two nodes) increases as these defects may be masked during the test phase [6], [9]. The Read or Write failure probability gets worse in the presence of short defects [7]. This makes the resistive-short defect a serious reliability issue, which must be considered in the test process of the STT-MRAM.

In the case of strong faults, one may use conventional logic-based test approaches, such as March tests, where the detection is performed by applying a sequence of write and read operations [7], [8]. These approaches are fault-oriented tests where the logic outputs of the main circuit are compared to the expected ones [6]. Normally, these approaches guarantee the detection of all the manufacturing defects (no test escapes) with the operation overhead of several read/write cycles. In the case of weak faults, which test escapes are likely, one requires additional circuits, such as a Design-for-Testability (DFT) circuit in order to decrease the number of test escapes [8]. These techniques provide a defect-oriented test approach which is applicable for detecting both weak and strong faults. In a defect-oriented test, we only monitor a parameter like current to detect a defect, without observing the logic output [10], [11].

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Some prior art references have proposed the fault modelling and related test approaches to cover the resistive defects in memory cells (e.g., [6], [9]–[12]). A test approach to detect resistive open defects of SRAM cell with adopted fault models was presented in [6]. The short defect models of CMOS SRAM were studied in [9]. In [10], a test approach to detect open and short defects of FinFET SRAM was described. Fault models and defect-oriented testing for Memristor arrays were studied in [11]. In [12], the authors proposed an effective test for the detection of the resistive short defects in CMOS circuits (including SRAM cells) based on the current consumption (I_{DDQ}). These test techniques may not be adequate for the STT-MRAM cells due to their different operation mechanisms and fabrication processes [7], [13]. More recently, some works including [7] and [8] have addressed defect and fault models for STT-MRAMs. In addition, a circuit-level approach to detect read disturb faults in STT-MRAM, based on monitoring the current during the read operation, was proposed in [14].

In nanoscale technologies, process variations adversely impact the effective operation of current-based tests [6]. It originates from difficulty in distinguishing between the defect or process variation as the origin of the current difference between the expected and the measured ones [6], [10]. The process variations exacerbate the detection range of resistive short defect that can be detected by a testing circuit [15], [16]. This necessitates the development of a robust testing methodology to detect the short defects of STT-MRAM in the presence of process variations.

In this paper, a defect-oriented test circuit is presented to detect faulty STT-MRAM cells caused by the short defects. The detection mechanism of the proposed DFT is based on the current difference between the currents flowing into and out of the cell generated by resistive-short defects in an STT-MRAM array. The technique detects both strong and weak faults. It is worth noting that the conventional testing approaches perform a set of read and write operations in a specified order to detect strong faults [8]. On contrary, the proposed DFT technique makes use of a single read operation to detect the faults. The main advantages of the technique include:

1) More accurate yield determination in terms of short defect detection compared to the conventional tests using the read/write operation.
2) Higher capability of strong defect detection in the presence of the process variation.
3) Better detection of weak defects which may escape from the conventional logic tests.

The rest of this paper is organized as follows. Section II reviews the STT-MRAM technology and describes the proper model for short defects to perform the test operation. The impact of short defects on STT-MRAM read and write characteristics, as the motivation behind the proposed technique, are discussed in Section III. Also, the details of the proposed test approach for detecting faulty cells in STT-MRAM array are explained in this section. In Section IV, the proposed test approach is assessed in the presence of process variation and the paper is concluded in Section V.

II. STT-MRAM Basics and Defect Modeling

In this section, details of the STT-MRAM cell as well as its read and write operations are presented. Also, the short defects modeling of STT-MRAM is briefly explained.

A. STT-MRAM Principles

Each bit cell of STT-MRAM consists of one MTJ as the storage device and one FinFET access transistor [2], [7]. A single STT-MRAM cell along with the conventional read circuit is shown in Fig. 1(a). In the STT-MRAM technology, the logical values '0' and '1', respectively, are stored in the form of parallel (P) or anti-parallel (AP) resistance state. The architecture of the memory array is shown in Fig. 1(b) that includes the STT-MRAM bit-cells and periphery circuits including the read/write circuitries [17]. Generally, three signals called bit-line (BL), source-line (SL), and word-line (WL) are utilized to perform the read and write operations of an STT-MRAM cell in the array [8].

B. Read and Write Operations

A column of the STT-MRAM is connected to the BL and SL of the read/write circuit and a stored data can be read or rewritten by activating the access transistor which is driven by WL [see Fig. 1(b)]. The three basic operations of STT-MRAM include read, write '0', and write '1'. As shown in Fig. 1(a), the reading operation of STT-MRAM is performed using a conventional sensing scheme consisting of sense amplifier (SA) and current-mirror-type load PMOS connected to the NMOS transistors [18]. The read circuit is enabled when the read enable signal (RE) becomes one. The resistance R_{ref} generates the current I_{ref} setting the voltage of one side of the current mirror to V_{ref}. The voltage of the other side of the current mirror is set to V_{cell} by the current I_{in} (the current flowing into BL) which is equal to I_{out} (the current flowing out of SL). Next, the Sense Enable (SE) signal in the SA circuit becomes one allowing the SA to amplify the difference between V_{cell} and V_{ref} to determine the state of the STT-MRAM cell. The signal V_{CLAMP} prevents the occurrence of unintended writes by limiting I_{ref}. In addition, the writing operation of STT-MRAM is performed using the write circuit presented in [19] by activating the write enable signal. The P (AP) state is written to the cell if *Data In* signal is 0 (1). During a write '0' operation, the write current flows from the BL terminal to SL. In contrast, for a write '1' operation, an opposite current is required to flow from the SL to BL through the MTJ device. To have a correct write operation, the transistors of the write circuit should be large enough to provide a sufficient amount of current.

C. Defects in STT-MRAM

One may classify memory faults into strong faults and weak faults depending on their detectability by normal read and write operations [8]. Strong deterministic faults, which always lead to logical faults, are easily detected by a sequence of read and write operations such as the March tests [8]. Random strong faults, such as Write Transition Fault, return a random

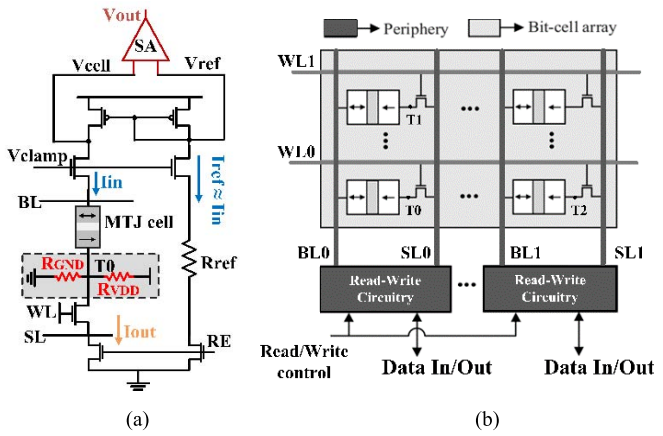

Fig. 1. STT-MRAM (a) bit cell with the read circuit and (b) array [7], [17].

value in the write operation, and hence their detections are not guaranteed by the March tests. In addition, the weak faults would cause parametric deviations which lead to reliability issues including higher failure rates or shorter lifetimes. These faults do not cause any logical faults. The inability to detect random and weak faults would classify them as hard-to-detect faults requiring additional DFT circuits or stress conditions for their detection.

In general, the defects induced by the fabrication process in a hybrid CMOS/FinFET memory cell can be modeled as resistive opens or shorts between the cell terminals [7], [11]. In the case of STT-MRAM, the majority of the manufacturing defects are modeled by resistive shorts [7]. Fundamentally, due to different fabrication and additional magnetic process in STT-MRAM [13], SRAM or Memristor fault models and even their test approaches are not normally applicable.

D. Modeling of Short Defects

In STT-MRAM cells, resistive short defects involving the internal nodes have significant effects on the read and write failures [7]. These defects can be modeled by a resistance which connects the main cell internal node ($T0$) to the power (V_{DD}) or ground (GND) terminals as highlighted by dashed line box in Fig. 1(a). This figure shows a general resistive model (R_{VDD} and R_{GND}) for the STT-MRAM cell to capture the behavior of realistic short defects. Both intra-cell and inter-cell defects may be very well modeled by the proposed resistive models utilized in this work. As examples, intra-cell short defects, such as $WL0$ *to* $BL0$ (i.e., short circuit between $WL0$ and $BL0$ terminals of the main cell in Fig. 1(b)), $WL0$ *to* $T0$, or $WL0$ *to* $SL0$ behave as R_{VDD} because $WL0$ becomes V_{DD} during the read operation. Similarly, inter-cell short defects can be modeled by setting the terminals of other cells to V_{DD} or GND. For example, when the $BL1$ terminal is set to V_{DD}, a short defect occurs between $BL0$ and $BL1$ (the BL terminal of the adjacent cell).

III. Motivational Study and Proposed DFT Approach

In the first two sections, we show the impact of the short defects on the read and write operations and address the limitations of the conventional test approaches. While, in the last two subsections, the principles behind the operation of the proposed DFT approach will be discussed.

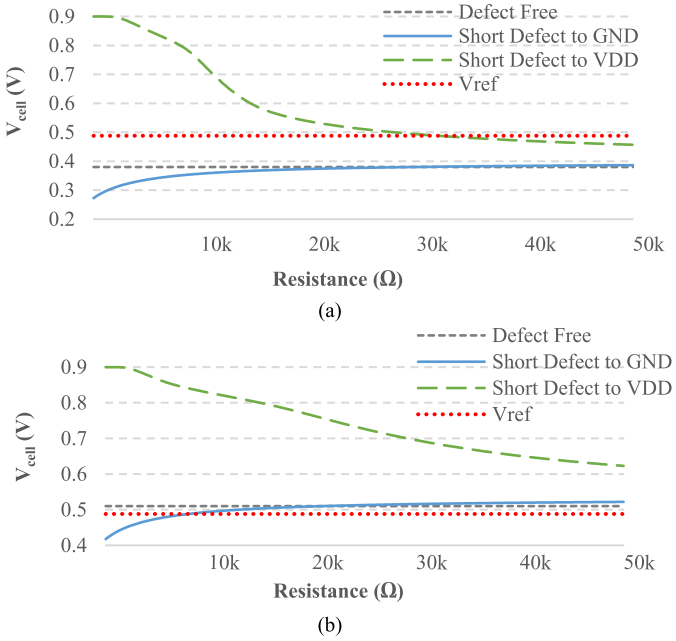

Fig. 2. V_{cell} in the (a) P-state and (b) AP-state during the read operation.

The impact of the short defects on STT-MRAM operations has been studied by implementing the MTJ component with a perpendicular magnetic anisotropy MTJ (PMA-MTJ) model from [20]. The PMA-MTJ has a lower switching current and a better scalability compared to the earlier in-plane MTJ [21]. The design parameters of MTJ were set using the parameters of [20] when considering the dimensions of 20 nm $\times$ 20 nm $\times$ 1.4 nm for width (W), length (L), and free layer thickness (T_m) of the MTJ, respectively. We also utilized the FinFET parameters of the PTM 20nm model [22] for the access transistor and peripheral circuits including the read and write circuits. The study was performed using HSPICE as the circuit simulator. The reference cell (R_{ref}) which resistance is the average of P- and AP- state resistances (i.e., $(R_P + R_{AP})/2$) was determined as 10 KΩ [18]. All circuit simulations were performed under the nominal supply voltage of 0.9V and the temperature of 25°C.

To consider process variations besides the short defects, we assumed a Gaussian distribution with the 3σ variation of 10% for the MTJ dimensions ($W \times L \times T_m$), 30% 3σ variation for the threshold voltage (V_{th}) and 10% 3σ variation for the length (L), fin thickness (T_{FIN}), and fin height (H_{FIN}) of the FinFET transistors. Note that variations of these parameters have the highest impact on read and write failure probabilities [2], [7].

A. Short Defects Impact on Read Operation

The STT-MRAM cell voltages (V_{cell}) for defect-free (healthy) and defective cells during the read operation at P- and AP- states, respectively, are shown in Figs. 2(a) and 2(b). The black dashed line in Fig. 2(a), (2(b)) refers to the defect-free cell voltage at the P- (AP-) state which is about 0.38V (0.51V). In the considered cell, the reference voltage for the read operation (V_{ref}) was 0.48V which is shown by

the red dotted line. According to the reading mechanism of STT-MRAM cell described in Section II-B, the read error occurs when $V_{cell} > V_{ref}$ in the P-state and $V_{cell} < V_{ref}$ in the AP-state. In case of the defective cell, the V_{cell} values in the P- /AP- states under the short defect modeled by R_{VDD} (R_{GND}) are shown by large, dashed green (solid blue) lines.

During the read operation, the read current flows from the BL to SL in order to sense the resistive state of MTJ (P- or AP-state) according to the explanation given in Section II-B. In the presence of short defects modeled by R_{VDD}, increasing the current injected to the internal node $T0$ results in increased V_{cell} through a decrease in R_{VDD} [Fig. 1(a)]. As Fig. 2(a) indicates, in the P-state, when $R_{VDD} < 32K\Omega$, fault errors ($V_{cell} > V_{ref}$) may be observed using the conventional logic tests whereas in the AP-state, shown by Fig. 2(b), no read error ($V_{cell} < V_{ref}$) is detected for the defects modeled by R_{VDD}.

Furthermore, in the case of short defects modeled by R_{GND}, Fig. 1(a) shows that in the read state, R_{GND} and the access transistor behave as two resistors connected in parallel. If the impact of the defects is modeled by a large R_{GND} resistance, no read error will occur. On the other hand, if it is modeled by a small R_{GND} resistance, their equivalent resistance and, in turn, V_{cell} will decrease. As shown in Fig. 2(a), in the P-state, R_{GND} does not have any adverse effects on the read accuracy (no read errors of $V_{cell} > V_{ref}$ is observed by R_{GND}). In the AP-state, however, Fig. 2(b) indicates that R_{GND} values smaller than 7KΩ cause read errors ($V_{cell} < V_{ref}$). The above discussion shows the difficulty of the conventional read test in detecting resistive short defects.

To consider the impact of the process variations on the read operation, we performed 1,000 Monte Carlo (MC) simulations and obtained the V_{cell} distribution. The histograms of V_{cell} for defect-free and defective cells at P-/AP-state read operations are depicted in Fig. 3. For this study, the worst case R_{GND} and R_{VDD} values of $7K\Omega$ and $32K\Omega$, respectively, were considered. These values were chosen as the detection threshold resistances to distinguish fresh (Defect Free) cells from the faulty ones (see Fig. 2). More specifically, if there is no process variation, in the P-state (AP-state), we should have 100% detectability for the defects associated with $R_{VDD} < 32K\Omega$ ($R_{GND} < 7K\Omega$). In Fig. 3, the threshold line (black dashed line) refers to $V_{cell} = 0.48V$ such that the read error occurs when $V_{cell} > V_{ref}$ in the P-state and $V_{cell} < V_{ref}$ in the AP-state. As shown in Fig. 3(a), in the P-state, R_{GND} does not lead to incorrect read implying inability to detect the corresponding defects while R_{VDD} has a weak detectability (∼24%). For the AP-state shown in Fig. 3(b), defective cells related to R_{VDD} and 15% of defective cells associated with R_{GND} may not cause incorrect reads, and hence, may escape the logic test. This study again shows that the detection capability of the conventional read operation is weakened further in the presence of the process variation.

B. Write Operation Under Short Defects

The write operations of STT-MRAM during $P \rightarrow AP$ and $AP \rightarrow P$ state transitions are asymmetric. More specifically, the write operation in the state transition of $P \rightarrow AP$ takes longer time than that of state transition $AP \rightarrow P$. Furthermore,

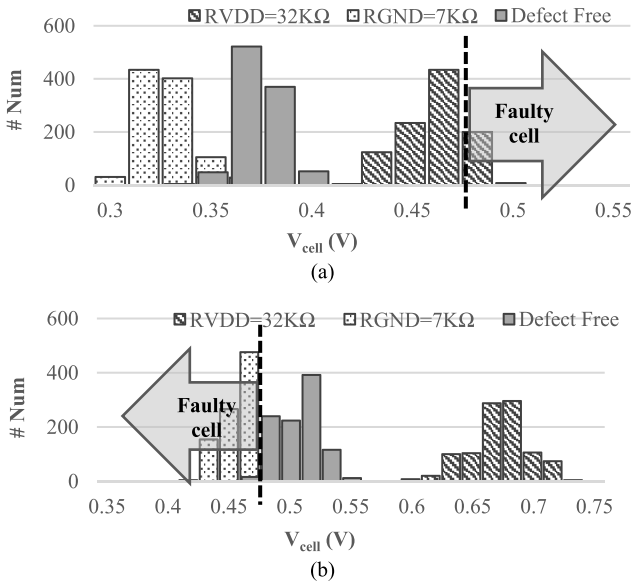

Fig. 3. Histograms of V_{cell} in the (a) P-state and (b) AP-state read operation.

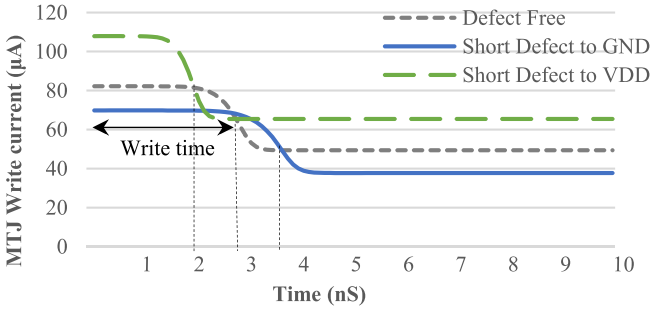

Fig. 4. The cell write time of $P \rightarrow AP$ transition.

the write operation for $P \rightarrow AP$ suffers from a larger switching time deviation (i.e., larger variation in the nominal required time for changing from P to AP) [23]. As mentioned in [23], the error rate (defined as the probability that the MTJ transition time is larger than the write pulse width) of the $P \rightarrow AP$ write operation is considerably larger than that of the $AP \rightarrow P$ operation due to a wider distribution of the MTJ switching time in the former operation for a given switching current. Thus, the limiting transition, in the STT-MRAM write operation, is the $P \rightarrow AP$ transition. The cell write time for the $P \rightarrow AP$ transition is plotted in Fig. 4, which shows that the write current (time) of a defect free cell is 51 μA (2.8 ns). For the $P \rightarrow AP$ state transition, the short defects modeled by R_{VDD} decrease the write time to 1.9 ns by supplying more current (i.e., 66 μA) to the MTJ. On the other hand, the short defects modeled by R_{GND} result in an increase in the MTJ write time to 3.7 ns due to a reduction in current flow (down to 39 μA) through the MTJ. In this case, the access transistor has to drive both the resistive defects and the MTJ cell. We considered a 10KΩ resistance for R_{VDD} and R_{GND} to perform the simulation of the write operation. This value is equal to R_{ref} (the average value of R_P and R_{AP}) to maintain the same distance from the P- and AP-state resistance values.

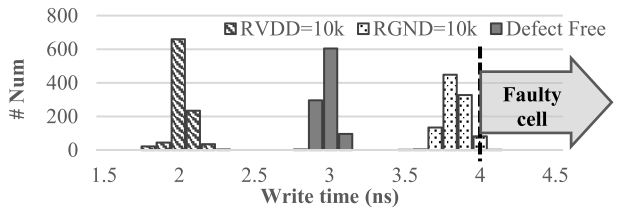

Fig. 5. Write time histograms for fresh and faulty cells in $P \rightarrow AP$ transition.

To detect an incorrect write operation due to a short defect, we define a threshold time which corresponds to the longest write time that a defect-free cell needs for the write operation to be completed under process variations. When the write time of a cell becomes larger than this threshold, we can conclude that the cell suffers from a defect. As mentioned in [23], the $P \rightarrow AP$ transition determines the timing threshold of the STT-MRAM write operation. In this work, this value is determined as 4 ns for the $P \rightarrow AP$ transition, which is slower than the $AP \rightarrow P$ write time margin (1.5 ns). Hence, a write fault occurs if the write time $>$ 4 ns.

In the case of $AP \rightarrow P$ state transition, R_{VDD} (R_{GND}) increases (reduces) the write time of the cell. It should be noted that none of the short defects can be detected using the $AP \rightarrow P$ write transition due to the fact that the write time alteration due to both R_{VDD} and R_{GND} defects are considerably smaller than the defined write time margin (< 4 ns), which is calculated based on the limiting transition of the STT-MRAM write operation (i.e., the write time of the $P \rightarrow AP$ transition). As mentioned before, the write time and the error rate of the $P \rightarrow AP$ write transition is considerably larger than that of the $AP \rightarrow P$ transition [23].

Now, let us illustrate the write time histograms for the defect-free and defective cells under the process variations. Fig. 5 shows the write time distribution for $P \rightarrow AP$ as the worst case using 1,000 MC simulations. In this study, as explained previously for Fig. 4, we considered R_{VDD} and R_{GND} as 10KΩ resistances and the write time threshold as 4 ns. As the figure reveals, the short defects modeled by R_{VDD} cannot be detected using a write logic test. Moreover, only 8% of the cells with short defects modeled by R_{GND} are detectable (the cells with the write time of larger than 4ns).

C. The Proposed Test Technique

In this section, we describe the principles of our proposed test technique. When there are no short defects, the currents flowing into BL (I_{in}) and out of SL (I_{out}) in a cell are the same. We used this property for our test technique. When there are any short defects, the currents are not the same [see Fig. 6(a)]. Let us denote this current difference by I_{diff}.

The currents I_{in}, I_{out}, and I_{diff} versus a range of R_{VDD} and R_{GND} defect sizes are plotted in Figs. 7(a) and 7(b). The results reveal that using I_{diff} is more effective in terms of short defect detection than considering either one of the other two currents (I_{out} or I_{in}). This current requires monitoring the values of I_{in} and I_{out} to distinguish the defect-free cells from the faulty ones. Fig. 7 shows that the detection of short defects with lower resistance values is easier than that of short defects

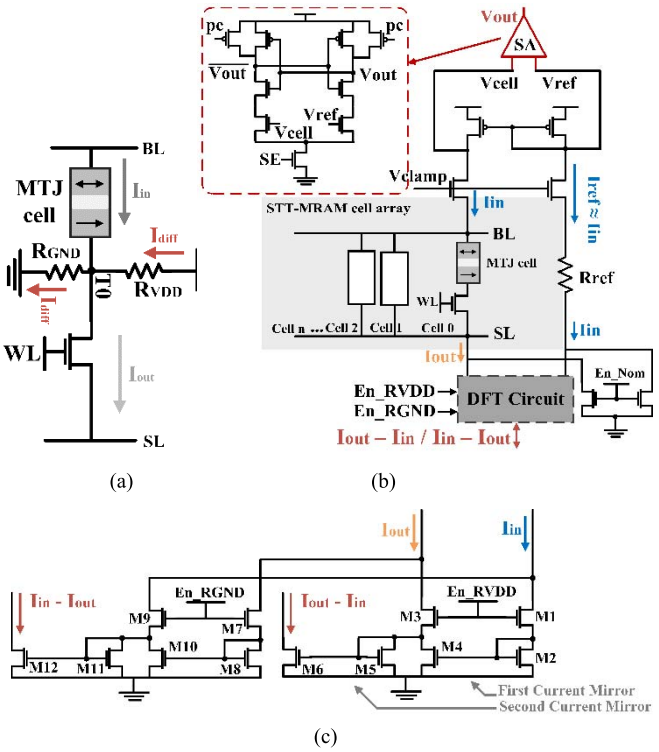

Fig. 6. (a) I_{diff} induced by short defects, (b) The modified read circuit, and (c) The proposed DFT circuit.

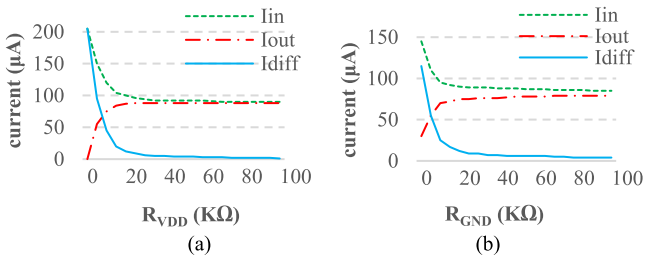

Fig. 7. I_{in}, I_{out}, and I_{diff} versus (a) R_{VDD}, (b) R_{GND}.

with larger resistance values due to higher I_{diff}. As examples, I_{diff} is 95μA (55μA) for the case of $R_{VDD} = 5k\Omega$ ($R_{GND} = 5k\Omega$) whereas it approaches zero when the resistance value is 100$K\Omega$. These figures also suggest that the short defects modeled by R_{VDD} are more detectable compared to the other ones owing to higher I_{diff} for the same resistance values. Finally, it should be noted that the technique provides wider defect detection ranges compared to the conventional tests (as will be inducted from the results of Section IV). For the considered STT-MRAM cell, we determine the feasible range of R_{VDD} and R_{GND} for the proposed DFT.

Finally, we study the robustness of testing based on I_{diff} in the presence of the process variations using 1,000 MC runs. Table I reports the variation of I_{in}, I_{out}, and I_{diff} for the short defects modeled by R_{VDD} and R_{GND} in the presence of the process variation. Simulation results in the table show that there are considerable variations for I_{in} and I_{out}. This implies that the conventional logic testing circuits which rely on monitoring a single current parameter (I_{out} or I_{in}) may not be very effective in determining the existence of the defects (especially

TABLE I
VARIATION OF THE I_{in}, I_{out}, AND I_{diff} UNDER SHORT DEFECTS

Short Defects	σ I_{in}	σ I_{out}	σ I_{diff}
To V_{DD} terminal	0.55 µA	0.531 µA	0.0187 µA
To *GND* terminal	0.531 µA	0.549 µA	0.0188 µA

for some weak defects) due to the larger current variation in the presence of process variations. The variation in the current difference value (I_{diff}) is much lower than I_{out} and I_{in} current values, offering more robustness against process variation when used as a parameter for the test. It should be mentioned that our results in Table I also show that 1,000 MC runs is large enough for the sample standard deviation to converge reasonably with an error of less than 2% ($\sigma/\sqrt{N}$) [24].

D. The Proposed DFT Circuit

The modified read circuit for a STT-MRAM array comprising n-bit cells is drawn in Fig. 6(b). This figure includes a conventional SA-based read circuit and the proposed DFT (shown by the dashed line box) which is designed based on the idea of monitoring I_{diff}. As shown in Fig. 6(c), we added 12 transistors to the conventional read circuit for implementing our proposed DFT. The proposed circuit has three operation modes:

1. Nominal mode (*En_RVDD/En_RGND* = 0, *En-Nom* = 1),
2. Short defect detection mode under R_{VDD} (*En_RVDD* = 1),
3. Short defect detection mode under R_{GND} (*En_RGND* = 1).

In the nominal (Defect Free) mode, which is activated by *En-Nom* signal, we utilize the normal operation of the conventional read circuit as explained in the Section II-B. In the two defect detection modes, one of the two signals *En_RVDD* or *En_RGND* becomes one so as to activate the DFT circuit shown in Fig. 6(c). The circuit measures one of the current differences of ($I_{out} - I_{in}$) or ($I_{in} - I_{out}$) to observe the effects of short defects on the array operation. For example, to detect short defects modeled by R_{VDD}, a differential current amplifier consisting of the right six transistors of M1-M6, enabled by *En_RVDD* signal, is employed to measure ($I_{out} - I_{in}$). In this case which I_{out} is larger than I_{in}, I_{in} (which is almost equal to I_{ref}) flows through the transistors M1 and M2 and then the value of I_{in} is copied to transistor M4 using the first current mirror circuit. On the other hand, I_{out} passes through M3 which generates the current difference of ($I_{out} - I_{in}$) for the transistor M5. The second current mirror copies the difference as the output current of the amplifier to M6. Similarly, the left 6 transistors of M7-M12 detect the short defects modeled by R_{GND} by measuring ($I_{in} - I_{out}$), where a similar explanation applies.

IV. RESULTS AND DISCUSSION

In deeply scaled technology nodes, the process variation greatly impacts the proper operation of circuits including the memories [15]. In this section, we investigate the effect of the process variations on the proposed DFT scheme. For this purpose, we performed 1,000 MC simulations and obtained the

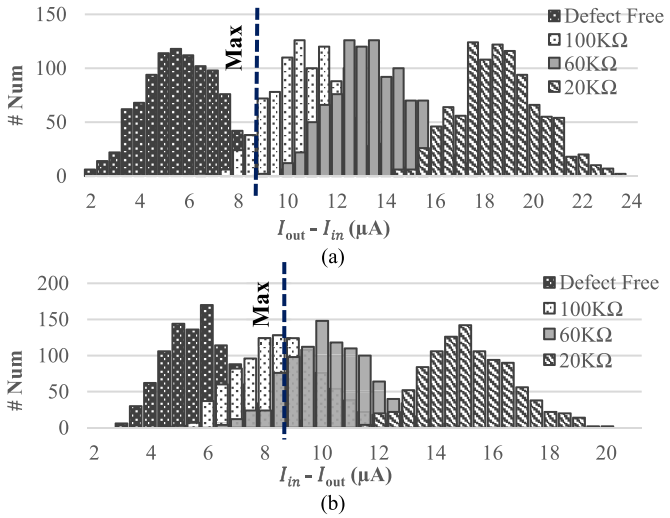

Fig. 8. The current difference histograms under the short defect to (a) V_{DD} and (b) GND terminals.

histograms of the current difference measured by the proposed DFT for the resistance values of 0, 20KΩ, 60KΩ, and 100KΩ as potential feasible values for R_{VDD} and R_{GND} (see Fig. 7). In the proposed DFT, the maximum I_{diff} value of the defect free cell, shown by the MAX lines in Fig. 8, is defined as the threshold to distinguish the fresh cells from defective ones. The results, which are plotted in Fig. 8, indicate that the proposed DFT circuit can detect short defects when the current difference is higher than this threshold which is 8.5 µA. These figures also show that the current difference makes the detection of the short defects easier (which means higher defect detectability) compared to the conventional tests (see Figs. 2, 3, and 5), especially, for smaller resistance values. For instance, in the case of 20 KΩ and also smaller resistance values, the defects modeled by both R_{VDD} and R_{GND} may be fully detected by the proposed technique. As can be observed from Figs. 2, 3, and 5, however, the conventional tests may not detect some short defects (see Sections III-A and III-B).

Figs. 8(a) and 8(b) demonstrate that detecting the short defects modeled by R_{GND} is more difficult than detecting defects associated with R_{VDD}. As an example, in the case of R_{GND} = 100 KΩ (see Fig. 8(b)), there is a considerable overlap between the current distributions of the defect-free and defective cells which results in lower detection capability compared to the case of R_{VDD}. Nevertheless, the ability of the proposed DFT in detecting the short defects modeled by R_{GND} is significantly higher than that of the conventional tests (see Table II).

To have a better comparison, we have calculated the detection probability (P_{Detect}) of short defects by again performing 1,000 MC simulations for the conventional and the proposed DFT techniques under a wide range of R_{VDD} and R_{GND} resistance values. Table II shows the range of resistance values that can be detected fully ($P_{Detect} = 1$) or partially ($0 < P_{Detect} < 1$) by the proposed DFT compared to the conventional logic tests using the read and write operations in the presence of the process variation.

In the conventional test techniques, when the write time is greater than the largest write time ($P \rightarrow AP$) which is 4 ns,

TABLE II
DEFECT DETECTION RANGE FOR THE PROPOSED AND CONVENTIONAL LOGIC TEST TECHNIQUES

Short defects	Proposed	Read (P) (Conv.)	Read (AP) (Conv.)	Write (Conv.)
To V_{DD} (Fully)	0-100K	0-20K	X	X
To V_{DD} (Partially)	100K-10M	20K-50K	X	X
To GND (Fully)	0-50K	X	0-5K	0-100
To GND(Partially)	50K-4M	X	5K-50K	100-20K

a write fault is considered. Also, a read fault occurs when V_{cell} is higher (lower) than $V_{ref} = 0.48\ V$ for the P-state (AP-state). In the proposed DFT, a defect is detected when the current difference is higher than the maximum I_{diff} value (i.e., 8.5 μA). Table II indicates that for the defects modeled by R_{VDD}, the conventional technique, the read operation in the AP-state and also the write operation may not detect any defects. This type of defects is detectable in the range of 0-50KΩ using a conventional read operation when the cell is in the P state. Our proposed testing scheme can increase this detection range to 10MΩ. Furthermore, the conventional P-state read test cannot detect any defective cells modeled by R_{GND} whereas the detection range in the AP-state for the same test is for the defects causing resistance values of up to 50KΩ. The conventional write test can detect defects leading up to 20KΩ of R_{GND}. The proposed technique has the full (partial) detection range of 0-50KΩ (50K-4MΩ) which is at least 10 times larger than the maximum range of the conventional tests.

Finally, it should be mentioned that although the conventional test circuits do not need any additional transistors, the proposed DFT technique requires 12 extra for a column of STT-MRAM array [see Fig. 6(c)]. This is, however, not a major setback because as the memory size get larger, the percentage of area overhead of the DFT circuit decreases. For instance, it become $\sim$1% for a column of 2Kb STT-MRAM cells.

V. CONCLUSION

In this paper, we proposed a defect-oriented testing scheme to detect the short defects present in STT-MRAM cells. The scheme had the ability to detect some of the defective cells which escaped the conventional logic tests. The short defects of STT-MRAM were modeled as R_{VDD} and R_{GND} which connect the internal node of the memory cell to the power terminals. The proposed DFT circuit worked based on the current difference observed between input current to and output current from the cell. The proposed test circuit had better robustness under process variations. To compare the detection probabilities under process variations, we performed 1,000 Monte Carlo simulations using HSPICE. The results showed that the proposed testing scheme improved the detection range of short defects modeled by the resistance to the ground (supply voltage) terminals by at least ten (five) orders of magnitude when compared to the maximum detectable defect sizes using conventional logic-based tests. Also, the area overhead was negligible for larger memory arrays ($\sim$1% for a 2Kb array). The proposed DFT enjoys from a single read operation compared to the several read/write sequences required for conventional approaches such as March tests.

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