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Shrinking FPGA Static Power via Machine Learning-Based Power Gating and Enhanced Routing

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Abstract

Despite FPGAs rapidly evolving to support the requirements of the most demanding emerging applications, their high static power consumption, concentrated within the routing resources, still presents a major hurdle for low-power applications. Augmenting the FPGAs with power-gating ability is a promising way to effectively address the power-consumption obstacle. However, the main challenge when implementing power gating is in choosing the clusters of resources in a way that would allow the most power-saving opportunities. In this talk, the design challenges and important requirements of power gating technique will be discussed in detail. Then we will introduce our proposed solutions to tackle these challenges. In this regard, we take advantage of machine learning approaches, such as K-means clustering, to propose efficient algorithms for creating power-gating clusters of FPGA routing resources. In the first group of proposed algorithms, we employ K-means clustering and exploit the utilization pattern of routing resources. In the second group of algorithms, we enhance the power-gating efficiency by minimizing the power overhead introduced by power-gating logic and by taking into account the size of routing multiplexers, which influences the power-gating efficiency. Finally, we enhance and further develop the baseline FPGA routing algorithm to be aware and take advantage of power gating opportunities.

Biography

Zeinab Seifoori received her Ph.D. and M.Sc. degrees in computer engineering from the Department of Computer Engineering at Sharif University of Technology, Tehran, Iran, under the supervision of Dr. Hossein Asadi and Dr. Amir Hossein Jahangir, respectively. She was a member of the Network and Data Communication Lab, SUT, where she worked on real-time wireless sensor networks. In 2015, she joined Data Storage, Networks, and Processing (DSN) Lab, SUT, where she worked on improving the efficiency of routing networks in configurable devices. As a research intern, she visited the Parallel Systems Architecture Laboratory (PARSA-Lab) at (EPFL) from March 2019 to March 2020. Her research interests include low power design, Reconfigurable Computing, Machine Learning, and Neural Networks.

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