پژوهشگاه دانش‌های بنیادی
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سخنرانی علمی

Design Challenges of Mixed-Criticality Systems

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دانشگاه صنعتی شریف

Abstract

An increasingly dominant trend in designing real-time and embedded systems is the integration of functionalities with distinct criticality levels onto a shared hardware platform. Criticality is the determination of the level of assurance against failure needed for a system component. A Mixed-Criticality System (MCS) is one that has two or more different levels. A well-known MCS is a dual-criticality system that is composed of low-criticality and high-criticality tasks. The complex embedded systems found in the automotive and avionics industries are evolving into MCSs in order to meet stringent non-functional requirements relating to cost, space, weight, heat generation and power consumption. As the shared platforms of MCSs are migrating from single cores to multi-cores, the availability of multiple cores on a single chip provides opportunities to employ fault-tolerant techniques to ensure the reliability constraints of MCSs. However, applying fault-tolerant techniques will increase the power consumption on the chip, and thereby on-chip temperatures might increase beyond safe limits. To prevent thermal emergencies, urgent countermeasures, like Dynamic Voltage and Frequency Scaling (DVFS) or Dynamic Power Management (DPM) will be triggered to cool down the chip. Such countermeasures, however, not only may lead to suspending low-criticality tasks, but also may lead to violating timing and reliability constraints of high-criticality tasks. Therefore, guaranteeing the timing and reliability constraints of high-criticality tasks, maximizing the Quality of Service (QoS) of low-criticality tasks, and meeting the power/energy and temperature constraints of the system are important challenges in designing MCSs. In this talk, the design challenges and important requirements of mixed-criticality systems will be introduced in detail. Moreover, some proposed solutions to tackle these challenges will be discussed.

Biography

Sepideh Safari received the M.Sc. and Ph.D. degrees in computer engineering from Sharif University of Technology, Tehran, Iran, in 2016 and 2021, respectively. She was a visiting researcher in the Chair for Embedded Systems (CES), Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, from 2019 to 2021. Her research interests include: scheduling of real-time mixed-criticality embedded systems, low-power design of embedded and cyber physical systems, energy management in fault-tolerant mixed-criticality systems, and multicore systems with a focus on dependability/reliability.

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