پژوهشگاه دانشهای بنیادی
پژوهشکده علوم کامپیوتر

IPM

"سخنرانی‌های علمی"

TAMA: Turn-aware Mapping and Architecture "A Power-efficient Network-on-Chip Approach"

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پژوهشگر پسادکترا در پژوهشگاه دانش‌های بنیادی (IPM)

Abstract

Nowadays, static power consumption in chip multiprocessor (CMP) is the most crucial concern of chip designers. Power-gating is an effective approach to mitigate this issue. Network-on-Chip (NoC) as the backbone of multi- and many-core chips has no exception. Previous state-of-the-art techniques in power-gating desire to decrease static power consumption alongside the lack of diminution in performance of NoC. However, maintaining the performance and utilization of the power gating approach has not yet been addressed very well. In this work, we propose TAMA (Turn-Aware Mapping & Architecture) as an effective method to boost the performance of the TooT method that was only powering on a router during turning pass or packet injection. By employing metaheuristic approaches (Genetic and Ant Colony algorithms), we develop a specific application mapping that attempts to decrease the number of turns through interconnection networks. Accordingly, the average latency of packet transmission decreases due to fewer turns. Also, by powering on turn routers in advance with lightweight hardware, the latency of sending packets diminishes.

Biography

Mohammad Baharloo is a Postdoc fellow at the Institute for Research in Fundamental Sciences (IPM). He received his Ph.D. degree in computer engineering from University of Tehran. His research interests include chip-scale wireless/photonic communications, performance modeling/evaluation of network-on-chip, high-performance and low-power multi/many-core processors, and hardware accelerators for machine learning.

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