پژوهشگاه دانشهای بنیادی
پژوهشکده علوم کامپیوتر

IPM

"سخنرانی‌های علمی"

Simultaneous Power Reduction and Aging Mitigation in Processors

نظام رهبانی

پژوهشگر پسادکترا در پژوهشگاه دانش‌های بنیادی (IPM)

Abstract

By increasing the popularity of battery-based processing systems, power management techniques have become mandatory for an acceptable operation time of the system with a single battery charge. On the other hand, by entering the nano-scale fabrication technology era, the lifetime of chips are strongly limited due to aging. Aging process gradually shifts the nominal parameters of transistors and other components in a chip, which lead to increase in transient or even permanent faults rate. To mitigate aging rate, different techniques are applied, which the simplest one is guardbanding. In this technique a guard-band is considered for operating voltage and frequency of chip. However, this technique diminishes the benefits of entering smaller feature-size technologies, thus, more intelligent aging mitigation techniques are in the highest demand.

In this talk we will take a look at the most famous aging processes and one of the techniques we proposed for simultaneous power and aging reduction of on-chip memories. Furthermore, we will take a look at one novel aging assessment technique to assess aging rate in processors with the least performance and area overheads.

Biography

Nezam Rohbani received his B.Sc. in computer engineering from Mazandaran University. He earned his M.Sc. focusing on energy-harvesting wireless sensor networks and his Ph.D. on aging-resistant processors from Sharif University of Technology. Now he is a postdoctoral researcher in Institute for Research in Fundamental Sciences (IPM), researching on low-power on-chip memories and aging assessment techniques for nano-scale chip fabrication technologies.

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