پژوهشگاه دانش‌های بنیادی
پژوهشکده علوم کامپیوتر

# سخنرانی علمی

# Multiple Network-on-Chip as A Power Efficient Chip Communication Infrastructure

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**Abstract**

Applying power gating on network-on-chip (NoC) as an effective static power-aware technique could lead to a significant reduction in on-chip network performance. Since the NoC performance has a considerable impact on the overall chip performance, providing a tradeoff between chip power and its performance is crucial. To this end, applying power gating in multiple network-on-chip (multi-NoC) instead of traditional NoC is a promising solution. However, in multi-NoC, waking-up a chain of routers in a switched-off sub-network (subnet) incurs performance penalty. By providing an opportunity to change the subnet of packets in multi-NoC architecture it can be avoided that packets encounter switched-off routers which improves the efficiency of power gating technique.

**Biography**

Mohammad Baharloo is a Postdoc fellow at the Institute for Research in Fundamental Sciences (IPM). He received his Ph.D. degree in computer engineering from University of Tehran. His research interests include chip-scale wireless communications, performance modeling/evaluation of network-on-chip, high-performance and low-power multi/many-core processors, and hardware accelerators for machine learning.

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