Design of Efficient Logic Circuits Using Magnetic Tunnel Junction Cells (MTJs)

By: Dr. Mahdi Fazeli
Iran University of Science & Technology

Abstract

CMOS technology is the dominant semiconductor technology for microprocessors, memories and application specific integrated circuits (ASICs). Some disadvantages of this technology include: long reboot latency of programmable circuits, data loss during unexpected power supply interruptions and high leakage currents, especially when the technology scales down to 100 nm and below. In order to improve the reboot speed, data security and reduce energy dissipation, recently, the design and implementation of circuits using Nano-scale magnetic cells is highly regarded. Nano-scale magnetic cells such as MTJs (Magnetic Tunnel Junction) are tiny, fast, programmable, non-volatile, almost zero static power consuming, and compatible with semiconductor elements. These special features have made MTJs a viable solution for future logic devices and memories. In this talk, I will introduce the previous and our proposed solutions for efficient design of logic circuits using MTJs.

Biography

Mahdi Fazeli received the M.Sc and Ph.D. degrees in computer engineering both from the Sharif University of Technology, Tehran, Iran, in 2005 and 2011, respectively. He has been with the department of computer engineering, Iran University of science and technology (IUST), since 2011, where he is currently an associate professor. He has established and chaired two research laboratories at IUST since 2012, namely Dependable Systems and Architectures Laboratory (DSA) and Networked and Embedded System Laboratory (NESL). He has authored and co-authored more than 60 papers in reputable journals and conference proceedings. His research interests include reliable issues in VLSI circuits and emerging technologies, dependable embedded systems, Low power circuits and systems, fault-tolerant computer architectures, fault injection and reliability modeling and evaluation.

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