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سخنرانی علمی

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Aggressive undervolting of FPGAs: Power and Reliability Trade-offs

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Abstract

This talk is about the experimental evaluation of aggressive undervolting, i.e., voltage scaling below the nominal safe level to reduce the energy consumption of Field Programmable Gate Arrays (FPGAs). Usually, voltage guardbands are added by chip vendors to ensure the worst-case process and environmental scenarios. Through experimenting on several FPGA architectures, we measure this voltage guardband to be on average 39% of the nominal level, which in turn, delivers more than an order of magnitude power savings. However, further undervolting below the voltage guardband may cause reliability issues as the result of the circuit delay increase, i.e., start to appear faults. We extensively characterize the behavior of these faults in terms of the rate, location, type, as well as sensitivity to environmental temperature, with a concentration of on-chip memories, or Block RAMs (BRAMs). Finally, we evaluate a typical FPGA-based Neural Network (NN) accelerator under low-voltage BRAM operations. In consequence, the substantial NN energy savings come with the cost of NN accuracy loss. To attain power savings without NN accuracy loss, we propose a novel technique that relies on the deterministic behavior of undervolting faults and can limit the accuracy loss to 0.1% without any timing-slack overhead.

Biography

Behzad Salami is a post-doc researcher in the Computer Science (CS) department of Barcelona Supercomputing Center (BSC). He received his Ph.D. in Computer Architecture from Universitat Politècnica de Catalunya (UPC) in 2018. Also, he obtained MS and BS degrees in Computer Engineering from Amirkabir University of Technology (AUT) and Iran University of Science and Technology (IUST), respectively. During his Ph.D. studies, he visited University of Manchester (UNIMAN) as a research internship student using a collaboration grant awarded from HiPEAC. He was/is involved in several H2020/FP7 EU-funded research projects including AXLE (Advanced Analytics for Extremely Large European Databases), LEGaTO (Low Energy Toolset for Heterogeneous Computing), and EuroEXA. His research interests are heterogeneous computing and low-power & fault-resilient hardware accelerators. More specifically, in his Ph.D. studies, he experimentally evaluated power consumption and reliability trade-offs of FPGAs through aggressive undervolting, i.e., underscaling the supply voltage below the nominal safe level. Findings of his recent work have been published in multiple conferences and journals such as Micro, FPL, PDP.

زمان : پنج‌شنبه ۹۷/۱۰/۲۰ – ساعت ۱۵

مکان : فرمانیه – خیابان شهید لواسانی – جنب برج کوه نور – نبش خیابان فربین – پژوهشگاه دانش‌های بنیادی – طبقه همکف

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