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Time-Based Computing with Stochastic Constructs

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Abstract

Stochastic computing (SC), a paradigm first introduced in the 1960s, has received considerable attention in recent years as a potential paradigm for emerging technologies and “post-CMOS” computing. In SC systems, logical computation is performed on random bit-streams. This offers some intriguing advantages over conventional binary radix. Complex functions can be implemented with simple hardware (e.g., multiplication using a single AND gate). This enables the design of low-area and low-power arithmetic units. Also, SC provides tolerance to soft errors, timing errors, and clock skew. The obvious disadvantage of SC is high latency. A stochastic representation is exponentially longer than conventional binary radix. Long latencies translate into high energy consumption and so offset any gains made by simplified hardware. We introduce a new, energy-efficient, high-performance, and much less costly approach for SC using time-encoded pulse signals. Implementation results show up to a 99% performance speedup, 98% saving in energy dissipation, and 40% area reduction compared to prior implementations. Circuits synthesized with the proposed approach can work as fast and energy-efficiently as a conventional binary design while retaining the fault-tolerance and low-cost advantages of conventional stochastic designs.

Biography

Dr. M. Hassan Najafi received the B.Sc. degree in Computer Engineering-Hardware from the University of Isfahan, Isfahan, Iran, the M.Sc. degree in Computer Architecture from the University of Tehran, Tehran, Iran, and the Ph.D. degree in Electrical Engineering from the University of Minnesota, Twin Cities, USA, in 2011, 2014, and 2018, respectively. He is currently an Assistant Professor with the School of Computing and Informatics, University of Louisiana at Lafayette, Louisiana, USA. His research interests include stochastic and approximate computing, unary processing, computer architecture, low power VLSI design, and designing fault-tolerant systems.

Dr. Najafi’s research establishes some counterintuitive, yet fundamental, new design methodologies for designing digital stochastic systems. Conceptually, his works challenge the limitations of bit-stream-based computing; practically, they provide a means for designing significantly smaller, faster, and energy-efficient embedded systems. In recognition of his research, he received the Doctoral Dissertation Fellowship from the University of Minnesota and the Best Paper Award at the 2017 35th IEEE International Conference on Computer Design (ICCD). His work on Polysynchronous Clocking was selected as the Feature Paper of the Month in the Oct 2017 Issue of the IEEE Transactions on Computers.

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