Normally-off Computing Architectures

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Abstract

One of the major challenges in device down-scaling is the increase in the leakage power, which becomes a major component in the overall system power consumption. One way to deal with this problem is to introduce the concept of normally-off instant-on computing architectures, in which the system components are powered off when they are not active. An associated challenge is the back-up and restoration of system states, which in turn can introduce additional costs that erode some of the gains. A promising alternative is the use of nonvolatile storage elements in the System-on-Chip (SoC) design which can instantly power-down and retain their values. In this talk, we discuss how we can design a normally-off SoC by exploiting non-volatile latches, flip-flops and registers. The idea is to design a hybrid architecture containing conventional CMOS bistables as well as different flavors of spintronic-based non-volatile storage elements, to balance performance, area, and energy efficiency.

Biography

Mehdi Tahoori is a full professor and Chair of Dependable Nano-Computing (CDNC) at the Institute of Computer Science & Engineering (ITEC), Department of Computer Science, Karlsruhe Institute of Technology (KIT), Germany. He received his PhD and M.S. degrees in Electrical Engineering from Stanford University in 2003 and 2002, respectively, and a B.S. in Computer Engineering from Sharif University of Technology in Iran, in 2000.
He holds several pending and granted U.S. and international patents. He has authored over 250 publications in major journals and conference proceedings. His current research interests include nanocomputing, reliable computing, VLSI testing, reconfigurable computing, emerging nanotechnologies, and systems biology. He has been a program and organizing committees of various conferences and symposia such as ITC, VTS, DAC, ICCAD, DATE, ETS, ICCD, ASP-DAC, GLSVLSI, and VLSI Design. He is currently the editor-in-chief of Elsevier Microelectronics Reliability journal, an associate editor for IEEE Design and Test Magazine (D&T), coordinating editor for Springer Journal of Electronic Testing (JETTA), associate editor of VLSI Integration Journal, and associate editor of IET Computers and Digital Techniques. He was an associate editor of ACM Journal of Emerging Technologies for Computing. He received a number of best paper nominations and awards at various conferences and journals, including ICCAD 2015, FPL 2017, and TODAES 2017. He was a recipient of the National Science Foundation Early Faculty Development (CAREER) Award.