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Circuit-Switched Memory Access NOCs for Servers

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Abstract

Emerging server workloads benefit from many-core processor organizations that enable high throughput thanks to abundant request-level parallelism. A key characteristic of these workloads is the large instruction footprint that exceeds the capacity of private caches. While a shared last-level cache (LLC) can capture the instruction working set, it necessitates a low-latency interconnect fabric to minimize the core stall time on instruction fetches serviced by the LLC. Today's many-core processors with a mesh interconnect sacrifice performance on server workloads due to NOC-induced delays. Low- diameter topologies can overcome the performance limitations of meshes through rich inter-node connectivity, but at a high area expense.

To address this problem, this work introduces CIMA – a hybrid circuit-switched and packet-switched mesh-based interconnection network that affords low LLC access delays at a small area cost. CIMA uses packet switching for short request packets, and benefits from circuit switching for long, delay sensitive response packets. While a request is serving by the LLC, CIMA attempts to establish a circuit for the corresponding response packet. By the time the request packet is serviced and the response gets ready, a circuit is prepared, and as a result, the response packet experiences little delay in the network. A detailed evaluation targeting a 64-core CMP reveals that CIMA reduces NOC delay by up to 15% over the state-of-the-art packet-switched router while increasing the area overhead by 2%.

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