Dynamic Heterogeneous Architecture in 3D to Address the Efficiency Crisis

By: Houman Homayoun
University of George Mason, USA

Abstract

3D die stacking is a recent technological development which makes it possible to create chip multiprocessors using multiple layers of active silicon bonded with low latency, high-bandwidth, and very dense vertical interconnects. 3D die stacking technology provides very fast communication, as low as a few picoseconds, between processing elements residing on different layers of the chip. The rapid communication network in a 3D stack design, along with the expanded geometry, provides an opportunity to dynamically share on-chip resources among different cores. This research describes an architecture for a dynamically heterogeneous processor architecture leveraging 3D stacking technology. Unlike prior work in the 2D plane, the extra dimension makes it possible to share resources at a fine granularity between vertically stacked cores. As a result, each core can grow or shrink resources, as needed by the code running on the core. This architecture, therefore, enables runtime customization of cores at a fine granularity and enables efficient execution at both high and low levels of thread parallelism. This architecture achieves performance gains of up to 2X, depending on the number of executing threads, and gains significant advantage in energy efficiency.

زمان : دوشنبه ۹۲/۰۴/۱۷ – ساعت ۱۶

مکان : فرمانیه – خیابان شهید لواسانی – جنب برج کوه نور – نبش خیابان فربین – پژوهشگاه دانش های بنیادی – طبقه اول

شرکت برای عموم علاقه مندان آزاد است